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Performance of PLD Grown ZnO Thin Film as a Thin Film Transistor

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PERFORMANCE OF PLD GROWN ZnO THIN FILM AS A THIN FILM TRANSISTOR

A Master's Thesis

Presented to

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In Partial Fulfillment

Of the Requirements for the Degree

Master of Science, Materials Science

By

Shahidul Asif

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Physics Astronomy and Material Science

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ABSTRACT

The performance of ZnO thin film (grown in different parameters) as a thin film transistor (TFT) is the focus of this study. ZnO is renowned for being n-type semiconductor naturally which was utilized in fabricating a thin film transistor here. This thesis is compared the performance of ZnO thin film transistor by growing the thin film using pulsed laser deposition (PLD) on two slightly different substrates at different temperatures in an optimal 0.1 milli bar oxygen pressure which was later analyzed using other material characterization methods. The substrates were both Si (100) but had different resistivity due to different amount of doping. The naturally oxidized silicon layer acted as the insulating di-electric layer between the substrate and the ZnO layer. The films were grown using the PLD with 20,000 laser pulses for each sample and one of them was annealed in the same oxygen environment to see the change in behavior as a device. The TFT's were fabricated as a bottom gated co-planar design and the samples were tested for output and transfer characteristics using a microprobe station in two different light exposure. The ZnO films were tested for structural and optical properties using X-ray diffraction and photoluminescence which gave important clues for explaining the device characteristics found in electrical characterization. The Raman and scanning electron microscopy were also performed for the samples which produced similar results for the samples. The best two samples were found where the ZnO was grown at 700 C and 500 C without annealing. They have the optimal oxygen vacancies for better transistor performance. On the other hand, the sample primarily grown at 350 C after initial 500 C base growth was inferior compared to the above-mentioned samples. The annealing was found to be detrimental to the TFT performance. Moreover, the substrate with minimal doping in silicon was found to be photosensitive giving a significant rise in channel current when exposed to the stronger light. The mobility of the two good samples of TFT was found in relevant range compared to the existing literature. The study would be more comprehensive with an inclusion of variation of oxygen pressure and different insulation layer with varying dielectric constant, which can be the future scope of this thesis.

KEYWORDS: thin film transistor (TFT), TFT channel, transfer characteristics, output characteristics, bottom gated TFT, co-planar TFT, pulsed laser deposition, photoluminescence

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I dedicate this thesis to my parents and to my wife Ira.

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INTRODUCTION

For the last fifteen years, ZnO has risen as a popular semiconducting material in the research of material science after it had a slowed down interest as so. ZnO was initially considered an alternative of GaN and other alloys as it is cheap and available in bulk, and the great optical performance as a strong luminescent while used as a pumped LASER. The attention was specially invested on the electrical properties and the tuning of the resistivity for the application as a suitable electronic and photonic device. The rare combination of high carrier (electron) mobility, good thermal conductivity, surprisingly large band gap, and specially the large exciton energy for binding buffering against the thermal energy make this material as a great candidate for application in thin film transistor and other electronic (diodes) and photonic (detectors, LED, LASER diodes) devices [1]. The major challenge has been the growth of a p-type material from ZnO which had rendered as a fast decaying, unstable, and difficult to control even it forms [2]. To achieve stable industrial applications, we need to have both the p-type and n-type nature of ZnO. Besides, the n-type ZnO are also not scrupulously explained how it behaves and why as the parameters are varied while growing the ZnO materials. Nevertheless, it is worth investing resource in delving the performance of ZnO based devices. The major catch of using ZnO over GaN and similar materials are the use of substrate. As the lattice mismatch of GaN with the most common sapphire is around 16% [3] and this results in more defect in the lattice which eventually make the device fabrication troublesome. Moreover, it is possible for applying superior quality wet etching on ZnO devices for fabrication, and it is also possible to tune the band gaps using Mg and Cd in the films/bulks [4]. These offered some tremendous flexibility in ZnO application in device engineering, and the study of ZnO became more and

more relevant.

In this study a big issue is probably the sensitivity of the performance of the film of ZnO as the impurity concentration changes. In the facility, the cleanliness is maintained as per the department standard, but this is probably not enough as even an impurity of 0.01 ppm can affect the conductivity which is especially crucial in the study of the performance of an FET and saturation achieving in the on region [5]. There was no clean room and the chamber facility had been shared by other workers for various materials' growth. This made some compromise in the electrical characteristics of the films, and the desired pattern of FET performance in plots are not achieved. Nonetheless, the films are grown in the same facility, and hence we can compare the parameters and output among them considering the flaws of the method.

The TFT is a direct derivative of an idea of the MOSFET technology with some structural changes. The operating principle is also very similar between these two, and thus in order to proceed a discussion and study of a TFT, it is relevant to understand the concept of the MOSFET which have been used in the industry for a long time [6]. Field effect transistor (FET) is a device which has three terminals (drain-source-gate), and the gate is electrically insulated from the main conducting channel hence it is an insulated gate FET. Usually a main n or p-type channel carries the main channel current, and an insulating layer keeps the gate separate electrically from the channel [7]. The resistance is usually in megaohm range and works as a capacitor. This high resistance keeps the gate to any terminal electrically impenetrable.

Now since there is no chance of any significant current to flow through the gate, the current through the channel is basically drawn by a potential difference between the source and gate. The voltage at the gate is the controller of the nature of the channel depth, cross section and the carrier concentration/mobility etc., and thus acting as a device controller. The amount of

charge due to the capacitance can affect the quality of the device, and thus it should be used or handled carefully lest it gets damaged electrically. The MOSFET operates in two different principles or modes which defines how the channel conduction works. If the FET channel is normally closed, and the gate voltage opens the channel, the device is depletion type. On the other hand, if the channel is switched on from the normally open channel, it is an enhancement type MOSFET (figure-1). Overall, the enhancement or the normally open channel is more efficient, and thus popular as it needs less power when off [8].

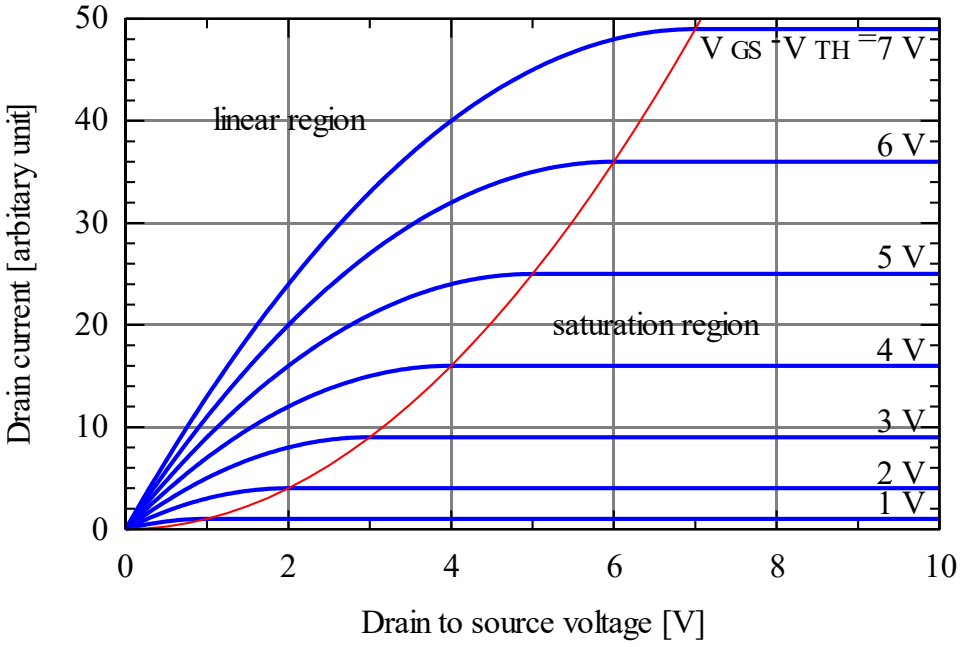

Figure 1: I_{DS}-V_{DS} curve of a MOSFET channel for different gate voltages, [9]

The channel consists of either electron or holes depending on the type of the material, and the metal oxide semiconductor FET uses the gate voltage to create an electric field to control the flow current (charge carriers) by creating conducting layers of electrons or holes. The MOSFET structure as we mentioned earlier has a drain and a source terminal which are two chunks of n-

type region (as the type of MOSFET, figure-2), and it stands on opposite p-type material standing on the substrate. The gate could be on top of the FET as separated by an insulating high-k material [8]. The voltage at the gate causes a conducting channel to emerge from the drain to source terminal, and the amount of gate voltage will determine the thickness of the layer.

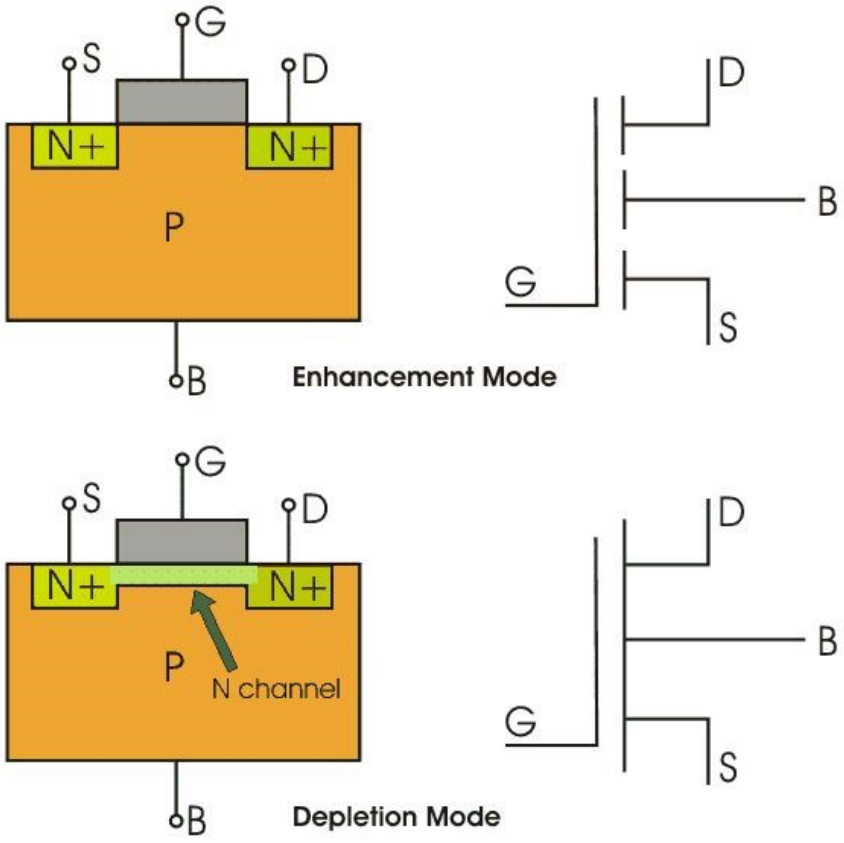

Figure 2: Structure of a generic enhancement and depletion type MOSFET, [8]

Again, if the drain voltage is higher than a particular amount, then it creates a depletion region at the drain's end, and the current will be saturated (figure-3) . Thus, before saturation the I-V curve between the drain and source will be ohmic, and after the saturation it is non-linear. Thus, it is used as a switch or enhancement of signal using the transfer characteristics [9].

A typical thin film transistor will have a channel between a drain and a source terminal and will have a gate for controlling the device. There are two main types of TFT as per the position of the drain and source terminals with respect to the channel. A coplanar TFT will have the terminals on one side of the channel, and the staggered TFT will have on different sides.

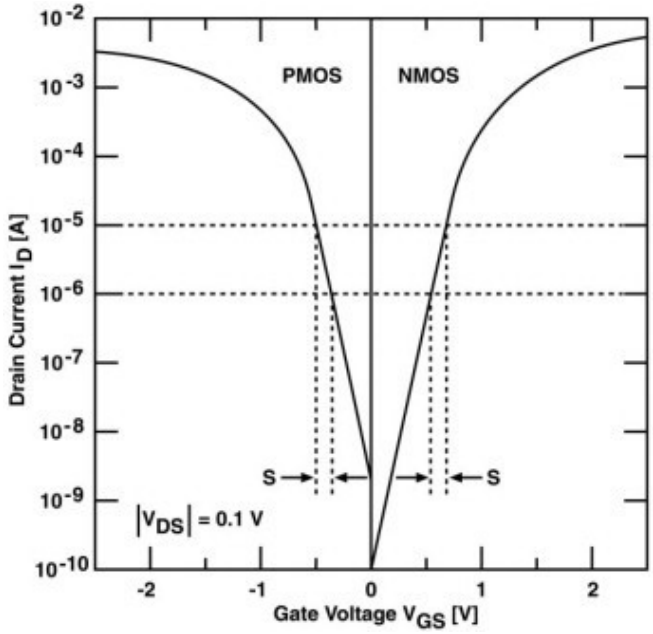

Figure 3: Impact of gate voltage V_{GS} on MOSFET characteristics, [9]

Again, the TFT can be divided into another two types as the gate's location on the device, being a top or bottom gated TFT. The operation MOSFET and the TFT are remarkably similar (figure-4), but still one has some advantages over the other depending on the contexts [10]. The TFT can be made on ridiculously cheap substrate making it easier to fabricate as typical glass or even plastic can act as one while the MOSFET may require fine expensive one crystal material for superior performance. This makes possible to produce flexible transistor application in display industry. Moreover, the TFT can be made well below the MOSFET's high thousand

Celsius growth temperature range making the technique simpler. The waiver of necessity of the both p and n-type junction is the most prominent as this advantage is applied in this study. The reason of this is the mechanism of conduction the two devices works on. The MOSFET needs an inversion layer whereas the TFT needs to build an accumulation layer needing only p or n-type material enough for working as a field effect transistor device [11].

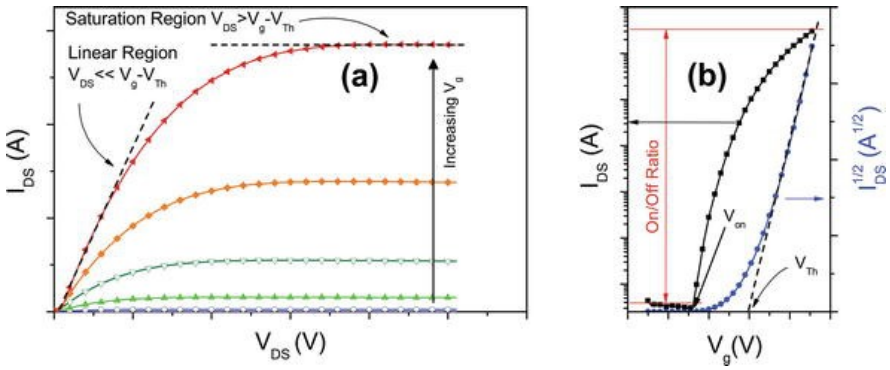

Figure 4: Relationship of I_{DS}-V_{DS} and I_{DS}-V_{GS} of ideal TFT, [12]

Now the channels conductance depends on the free charge carriers existing in the channel itself which otherwise controlled by the application of electric field at the gate (the gate voltage). Now as the semiconductor is of n-type in the TFT (as the ZnO is), an accumulation layer is developed by the free electrons (as the oxygen vacancy dictates) helping the conductivity [13]. If the negative bias is applied at gate electrode, the free electron will be repelled by the electric field, which will result in a minimal (often negligible) leakage current or noise in the channel depending on the TFT quality. The nature of output curve is mostly linear until the V_{DS} is beyond a certain limit when the pinch off occurs and the increment of the voltage will not contribute to the similar increase of the current increase and this is known as the saturation of the device [14]. There have been various TFT geometry using the metal oxide as an insulating dielectric layer

(figure-5), and the most common recently is the top gate geometry. This geometry is a little challenging to do when the laboratory is not very sophisticated, and it is always great to apply the back-gate geometry as for a starter for testing the effectiveness of the grown film. Hence this is used in the experiments. The electrodes were pure Au deposited by masked sputtering method, and it is applied since the lithography is not available in the PAMS lab. There are several great methods for producing good quality ZnO thin film. The best laser assisted method is the pulsed laser deposition (PLD). The MBE is a better method for fine quality ZnO film [15]. There are also several good chemical methods like sol-gel and spin coating which have been used successfully for thin film of ZnO. PAMS lab has a PLD chamber for growing films, and this is what is applied in the study. PLD is a popular method for growing ferroelectric, hard phases, polymers, compound semiconductors etc. from the eighties. It needs comparatively less temperature with a minimal mechanical and electrical sophistication. This thesis has its attention towards the performance of a FET based on ZnO grown on different growth parameters on the Si substrates. There were two substrates used for deposition of ZnO thin films, and they were tested for variations. We have known from the studies that the use of different substrates can change the nature of the crystallinity and the carrier concentration, and hence the FET performance. Again, varying the temperature and pressure can also change the characteristics of a ZnO thin film electronically and optically. The x-ray diffraction has been used for assessing the structural properties and this analysis gave an indication of the merit of the deposition of the thin films. Photoluminescence is a great tool for forecasting the nature of the film giving indications on vacancy ad interstitial properties which are the driving force of the behavior of a thin film as a semiconductor material. These two characterizations are the primary tools for explaining the behavior obtained in electrical characterization and using existing literature and journal some

analysis and explanation are drawn. The Raman analysis and SEM microscopy were performed to verify the thin films' deposition and stoichiometry, but they are not pivotal in playing the role of undoped ZnO on the same material substrate.

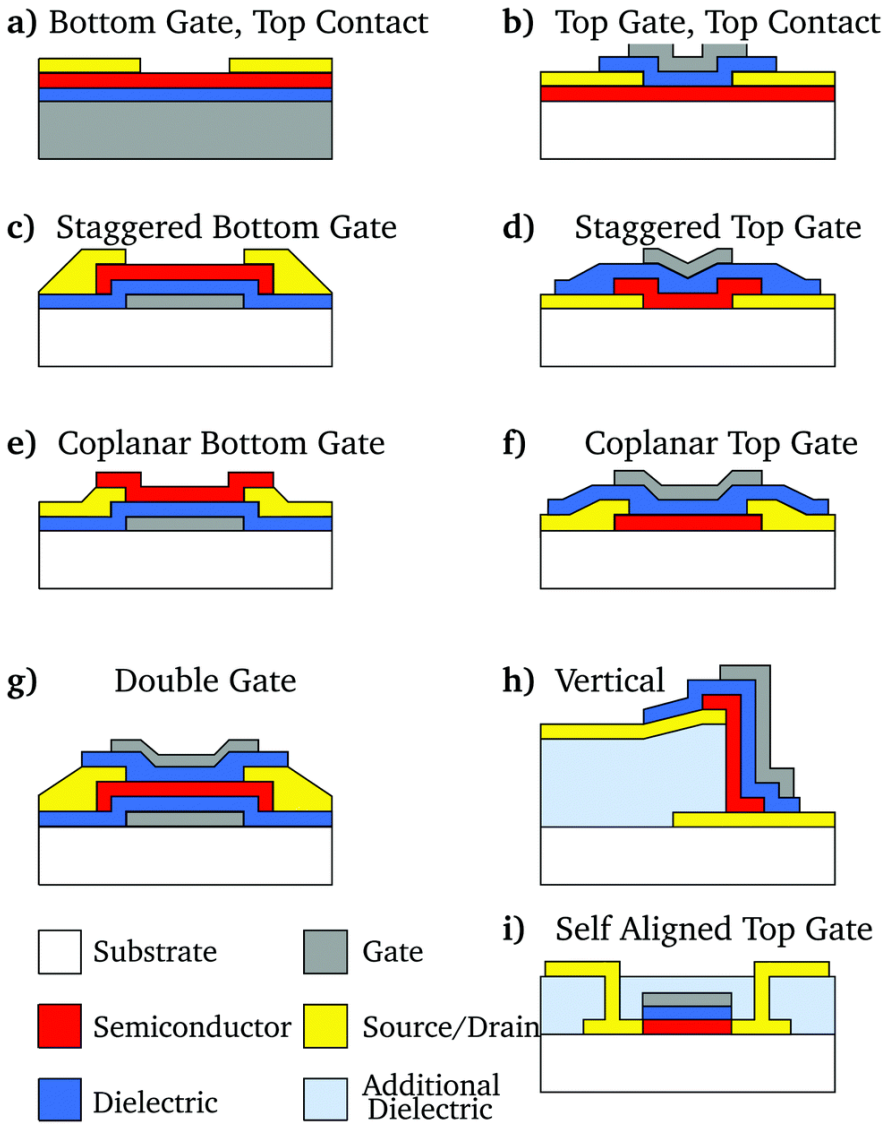

Figure 5: Generic structure of a TFT, [16]

METHODOLOGY

The substrate is an important element in the TFT (thin film transistor) performance and behavior. There are two Si wafer used as the substrate (figure-6), and they both are SiO_2/Si <100> orientation wafer. The main difference between them is the resistivity and hence the Si doping. The first substrate (substrate#1) was of around 200 Ω-cm of resistivity, and the second substrate (substrate#2) had only 0.1-0.5 Ω-cm of resistivity. The typical atmospheric oxidation of Si surface makes the substrate surface as a SiO_2 surface, and for the best interest of analysis, we

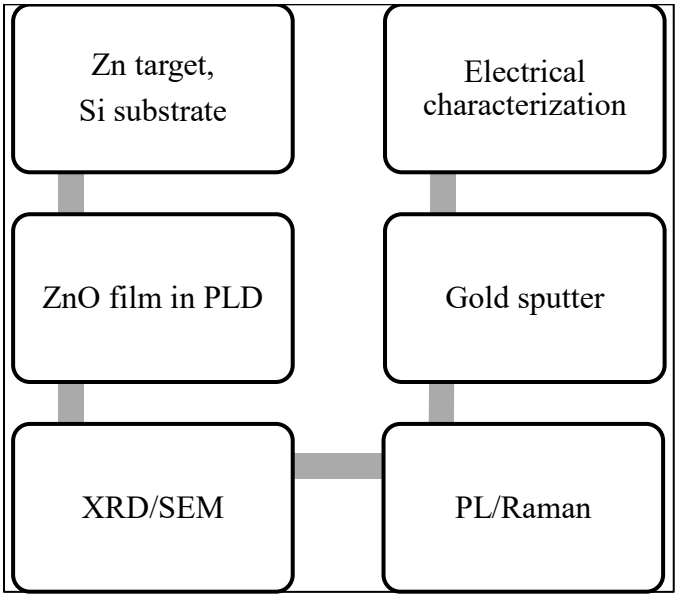

Figure 6: Steps of the experimental study

would etch the surface with HF to get a pure Si surface for the growth of thin film. For checking the performance, the first few samples were tested for the difference between etched and non-etched substrate, and the FET showed no significant difference in the performance. Now, as we know from previous studies that the thin SiO_2 layer over ZnO can be even used a FET [17]. As

we are using ZnO over the SiO_2 as a dielectric/insulator, we can safely use the substrate without etching, given the exposed rick of HF as a chemical, without any big compromise in the performance. Moreover, it is desired to have an insulator/di-electric layer between the substrate and the ZnO semiconductor layer for the best performance of a TFT.

There are mainly four/five cases studied: one in substrate#1 for 700 C growth temperature and three on the other substrate for three different temperature. The sample cases are tabulated (Table-1) for clarification. After doing the first deposition on the higher resistivity Si substrate at 700 C, the next one was done at 450 C. Next three samples were done on the second

Table 1: Samples in this study

	Sample#1	Sample#2	Sample#3	Sample#4	Sample#5
Substrate#	One	One	two	two	two
Temperature (C)	700	450	350-500	500	500
Pressure (mBar)	0.1	0.1	0.1	0.1	0.1
Anneal	no	No	no	no	30’ @500C

low resistivity substrate. The third sample has two temperature of growth in two stages. The initial few thousand shots are done at high temperature of 500 C, and then the most deposition was done at 350 C. The next sample was done only at 500 C while the last sample had 30 minutes of annealing at 500 C after being grown at the same temperature. The shots from the laser was around 20,000 shots.

The thin films were prepared using the pulse laser deposition method in a vacuum chamber under certain oxygen pressure (0.1 mBar) and substrate temperatures (as mentioned in

the table-1). A schematic diagram of the PLD is given in figure-7. The films are grown out of a Zn target place in the target holder in the chamber and using a LASER with wavelength of 266 nm. The laser is focused on the target through the window and the target is rotated using a carousel and stepper motor within a certain range of angle so that the target is

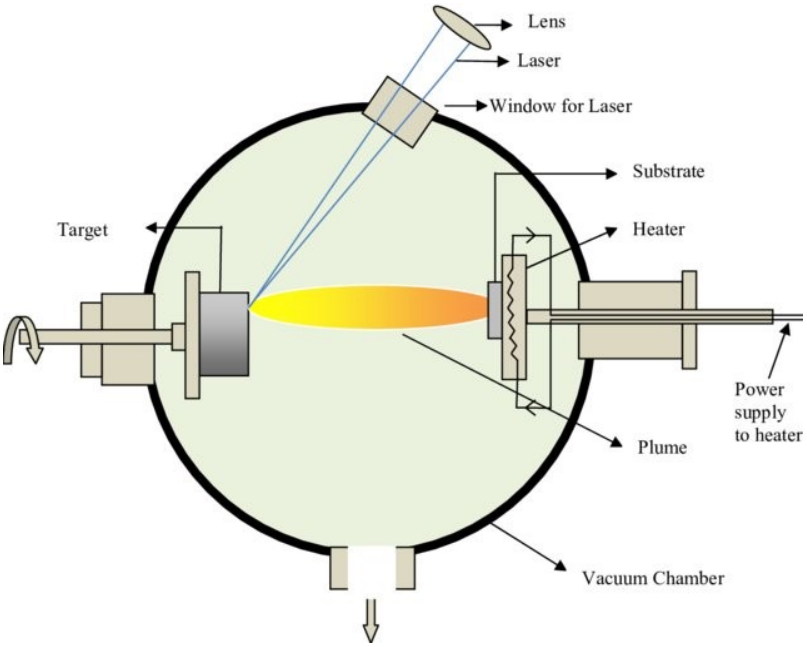

Figure 7: Generic Pulsed Laser Deposition chamber [18]

evenly used and not having a curved cavity and have a good performance in producing plumes. When the laser is incident upon the target, the Zn surface reaches thousands of Celsius in that point, and ablation occurs in the low-pressure oxygen environment creating a plasma plume which falls on the substrate holder and substrate. Before the actual ablation and deposition take place, the chamber is closed sealed airtight with the substrate holder with the substrate, and the chamber is sucked off the air to 10^{-5}mBar pressure before the oxygen gas is released in slow manner to make the chamber reach the desired pressure necessary. There is a substrate heater

controlled by a PID controller, and the thermocouple in the substrate holder measures the temperature of the substrate holder. It is necessary to keep the substrate at a high temperature for a good development of the layer on it (figure-8). After reaching the desired substrate temperature and the chamber pressure, the laser is turned on, and the first few hundred shots are fired in 10 Hz frequency using 120mJ laser energy with the shutter still over the substrate. Later the next 20,000 shots

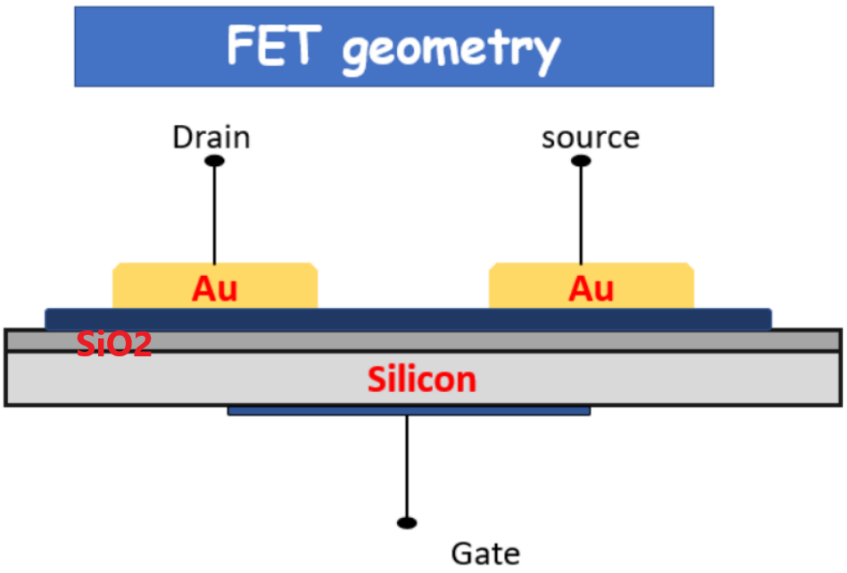

Figure 8: Schematic diagram of thin film transistor fabricated for this study

are fired after the shutter is removed, and the plume is to let on the substrate evenly. About half an hour of ablation later the laser is stopped, and the chamber is gradually taken into normal pressure by shutting down the pumps. The temperature of the substrate is allowed to decrease to room temperature, and the substrate is collected from the chamber with a thin ZnO film on it.

In recent decades, many types of growth method for a thin film on a surface are being widely used, and they are fallen into two main categories as physical and chemical methods.

They have their own merits as the ease of use, cost, quality and so on, and they are used as per the applications merit and nature. The physical [19] method is used for metal and alloys of which the MBE (molecular beam epitaxy) is the best and reliable method. It uses a controlled use of evaporation of targeted material and is controlled by a system to be in situ deposition in the chamber. This is a sophisticated method and needs a good controlled monitoring system for its efficacy. On the other hand, a method with less precision but easier control is proposed by using a laser incident on a target creating plumes to be deposited onto a film. This is known as a pulsed laser deposition (PLD) method, and it has way less maintenance and easier and quicker operation. This PLD method is applied for the growth of our film. The PLD provides a unique mean to achieve better multicomponent stoichiometric deposition with less complexity of the machinery. It also renders the low temperature option involving less corrosive gas, and no evaporation cells at all [20] Later the film will be used as device after electrodes put on it (figure-9).

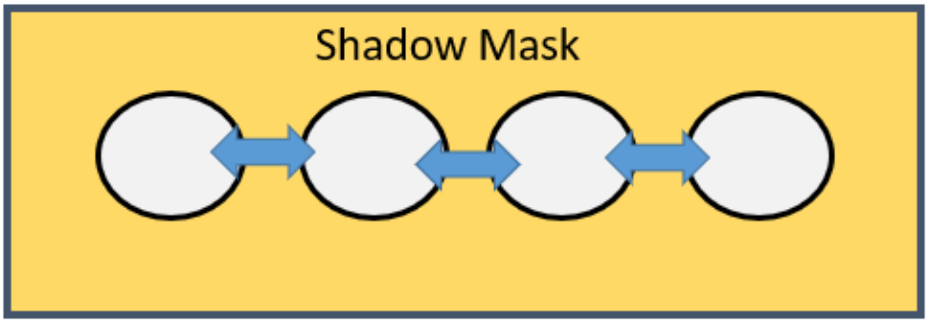

Figure 9:Shadow mask used for terminal electrode fabrication by Au sputtering method

The films after deposition are tested in x-ray diffraction (XRD) for desired crystallinity and if the desired peaks are achieved, the SEM/Raman/PL characterizations are performed for

further verification of ZnO thin film. The XRD was done using a Bruker Discover 8 Diffractometer instrument which has an alignment of the precision $\leq \pm 0.01°$ for the parameter 2Theta* over the desired range of angular motion. This instrument is known for the quality of maintaining linearity so that the XRD results are accurate, and the quality of data is reliable.

The Raman and photoluminescence spectroscopy were performed by Horiba Jobin Yvon LabRAM HR800` microscopes. For the scanning electron microscopy, FEI FESEM Quanta-200F was deployed for imaging and EDS study. Once these characterization results are obtained. the quality of the films is ascertained, and it undergoes the next step, the dot electrode making. A gold sputter machine is used for the fabrication of electrodes for the drain and source. The best method for fabrication of drain/gate electrode is the lithography, but as the PAMS lab does not have such a facility, the shadow masking is used for making electrodes. This method is not a full proof, and hence while the sputtering is done, the mask is ensured to be pressed enough to prevent the shorting of the terminals/electrodes while being fabricated which might happen if there is gap between the mask and the substrate. Once the electrode is fabricated the FET is practically ready for the electrical characterization (figure-10).

The gate is located at the bottom of the substrate and film. The drain and source are the two terminals fabricated on the ZnO film. These two terminals are similar and can be used interchangeably. Once we select the drain and source, the electrical connection can be made following the figure 10 The three quantities that matter is the current of the channel between the drain and source known as I_{DS}, the voltage between these two terminals known as $V_{DS,}$ and the voltage applied to the gate known as the V_{GS}. The ground the gate voltage and the source terminal are shorted as can be understood by the subscript. As we apply large enough gate voltage, the channel starts conducting creating a path from source to drain. The current and

voltage are measured by Keithley ammeter and voltmeter.

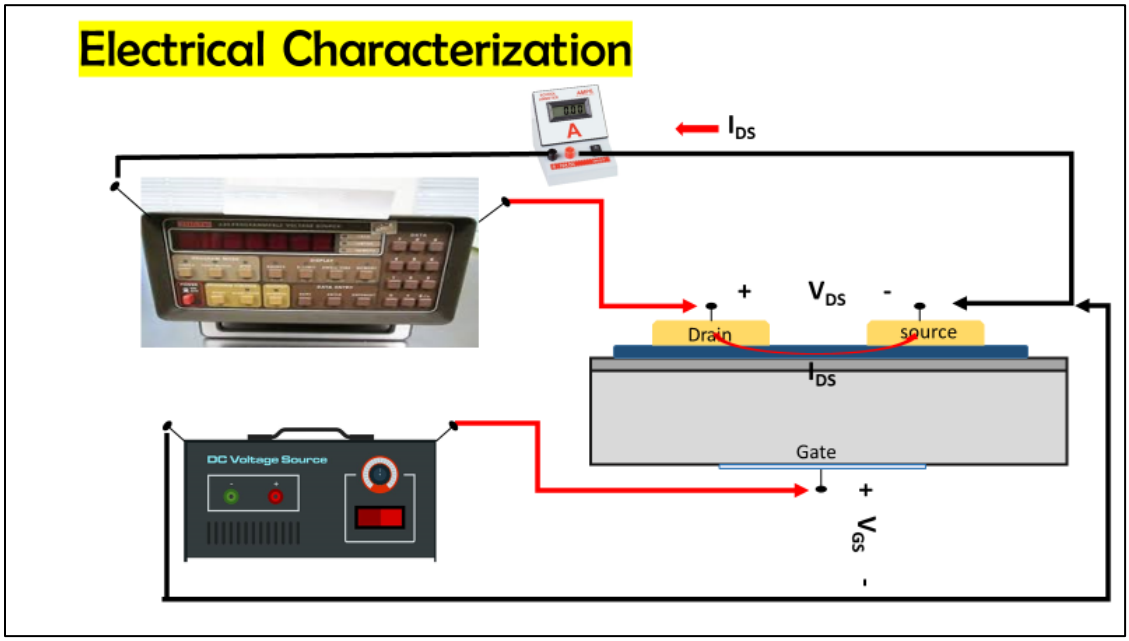

Figure 10: Schematic of experimental set-up of electrical characterization

RESULTS AND DISCUSSION

X-Ray Diffraction Study

There are several samples of film grown from Zn target to make a thin film of ZnO (figure-11) on Si substrate, and as mentioned before, the growth parameters are changed to inspect the changes of properties. The figures here will show the XRD analysis for different samples on different substrates

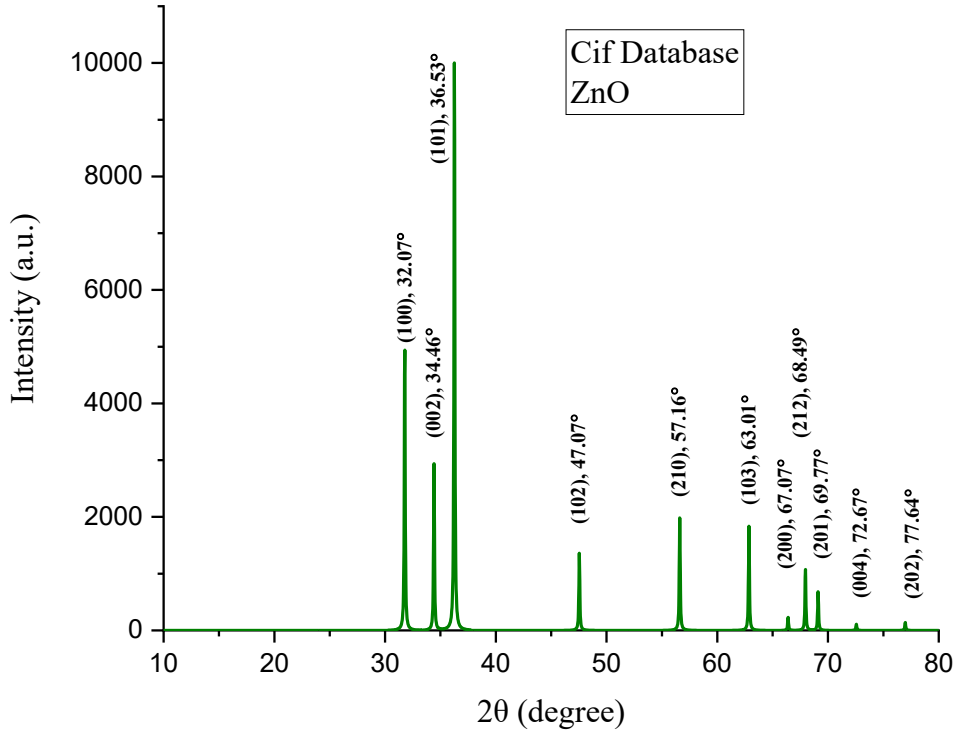

Figure 11: X-ray diffraction pattern from the cif file from database [21]

with varying growth parameters. They are discussed against their original cif files, the substrate peaks and among themselves. This will help studying the comparison among the growth

parameters and identifying the control factors which would eventually result in the performance as a FET fabricated from the oxide films.

Before describing the ZnO films grown in the lab, it is worth seeing the cif file as an XRD plot to expect what to see in a regular film of ZnO. Although the peaks given in a standard crystallographic file, will not necessarily come up in the film. On the contrary, there is a high probability of getting on or two dominant peaks if the films are grown as a preferred orientation crystal as usual films do. Most common peaks in the films are within the 30 to 50-degree ranges. There is also an effect from the substrate itself (figure-12), and it depends on the type of the substrate being used. The substrates those are used here are of Si (100) oriented crystal. They

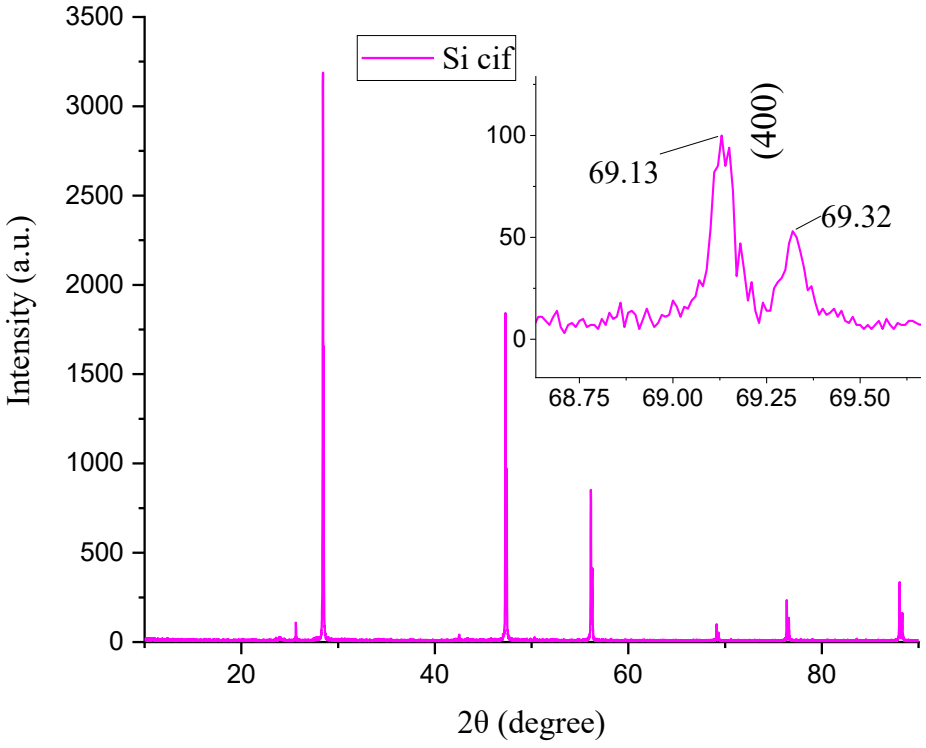

Figure 12: Si substrate peak in the prominent region [21]

have difference in the resistivity and doping, but since the doping is extremely low

concentration, apparently the crystallinity is not affected as much as the resistivity. Whenever the comparison and analysis are made, we have to consider the peaks those caused by the substrate itself. Figure 13 shows that the typical Si (100) substrate can produce a pair of peaks around 69° which represents (004) of the silicon bulk plane and this is what also expected from the substrates as well [19]. The peaks are distributed in the whole range of 2θ angle, but the preferred orientation is what gives us in only handful of peaks for a particular substrate. This will be

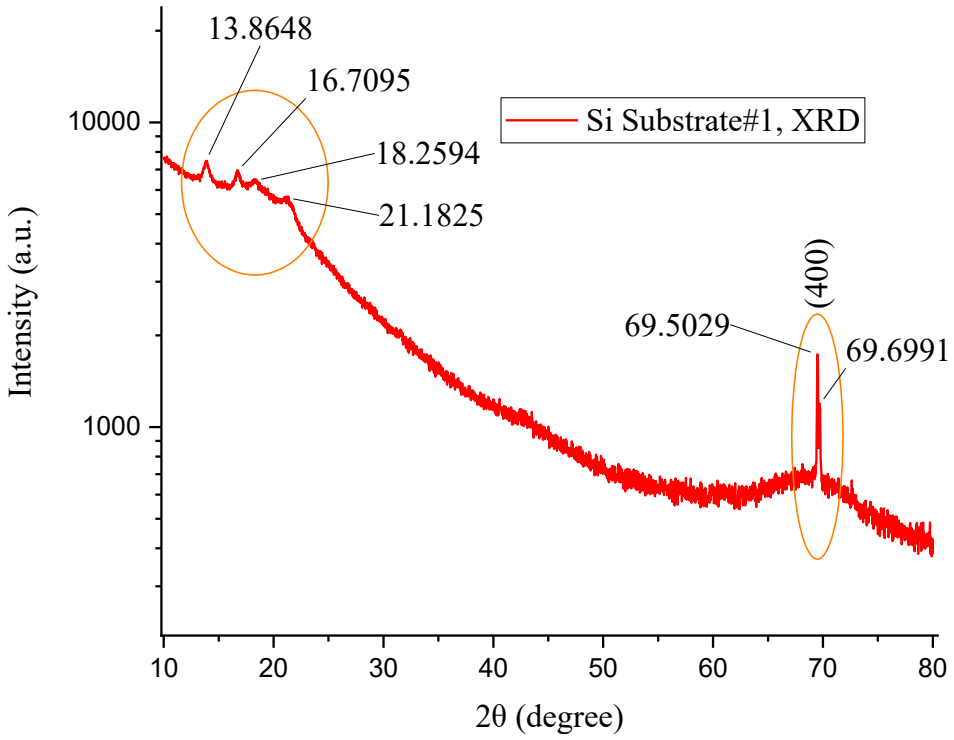

Figure 13: X-ray diffraction result of Si (100) Substrate#1

shown in the XRD plots of the substrate, and in the peaks obtained when the films are analyzed on the substrate. Figure 14 represents the probable peak range of the ZnO film deposited on the silicon substrate, and we can reckon that there are three zones of the prominent peaks. The early

zones are mild and relatively blunt, and a series of peaks can be noticed from the XRD patterns of this ZnO films. These two films are grown at 700 C and 450 C separately on the higher resistance substrate as mentioned earlier. The second zone is in the range of 30°-40° and has very prominent peaks with different magnitudes. At the end, we can notice some prominent peaks around 65°-75° range. Now, as we know these ranges, it will be easy for us to ascertain the sources of the peaks in the films or substrates or other impurities. To understand the peak generator materials, we should first study the substrate separately, so that it become easier to extract the substrate

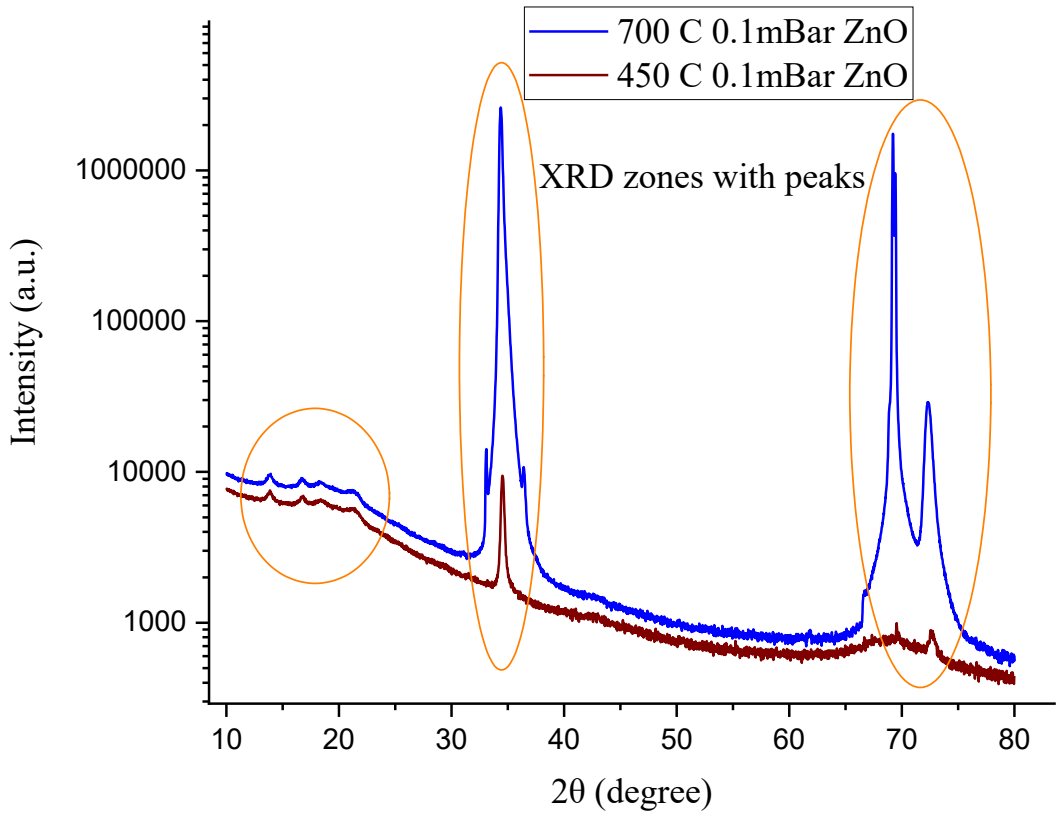

Figure 14: X-ray diffraction of the samples on 1st substrate (grown at 700 C and 450 C)

peaks of XRD from the sample and substrate peaks' mix. The plots of the substrate#1 give us a

clear indication that the initial range of peaks are present in the substrate XRD plots. It is also obvious that the mid-range zone is devoid of any peak in the substrate, and at the 60-70 zone, there are two prominent peaks existing in the plot of substrate. Apparently, these peaks should also be present in the whole samples XRD with some minor shifts and need to be ignored from the XRD plot to extract the ZnO peaks.

The plot of the ZnO grown at 700 C is having all the zones of peaks as mentioned. Obviously, it has the peaks of the lower angle zone as the substrate as shown in Figure 15. Hence

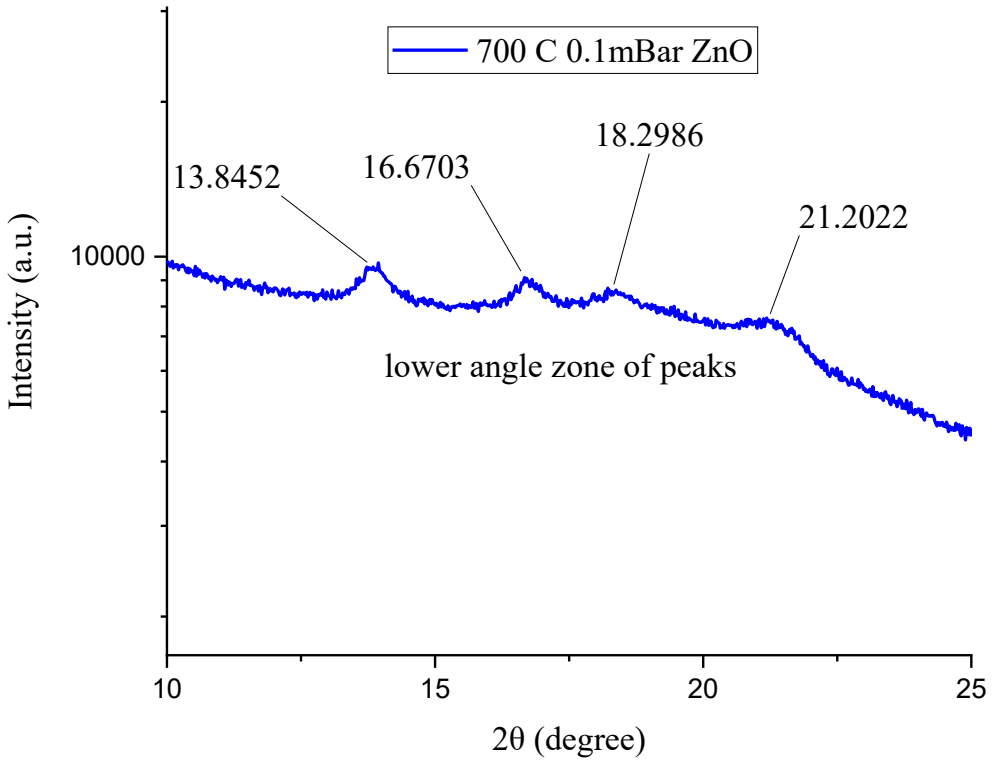

Figure 15: XRD peaks in early range of 2θ of sample grown at 700 C

these ae not from the ZnO film. Again, it also has the peaks around 69 degrees those come from the substrate. Hence these two should be ignored too. Now if we compare the magnitude of the

peak intensity for 700 C and 450 C, we can see that the peaks from the 700 C is much sharper (around 100-1000 times stronger), and thus the quality of the peaks and hence the film is also in better crystallinity in the 700 C sample.. Although the most prominent peak is the (002) peak at 34.35 degree, and this is the preferred orientation of this film which can be readily observed from the plot shown in Figure 16. In the XRD peak around 70-degree angle, there is a small peak which is of (004) plane of ZnO and definitely not from the substrate (figure-17). There are two mini peaks which can be seen in both side of this (002) peak, and they are (100) and (101) peaks at around 32.77 and 36.37 degree in the XRD plot. Now if we try to compare the plots of substrate and the ZnO film of 700 C (figure-18), we can

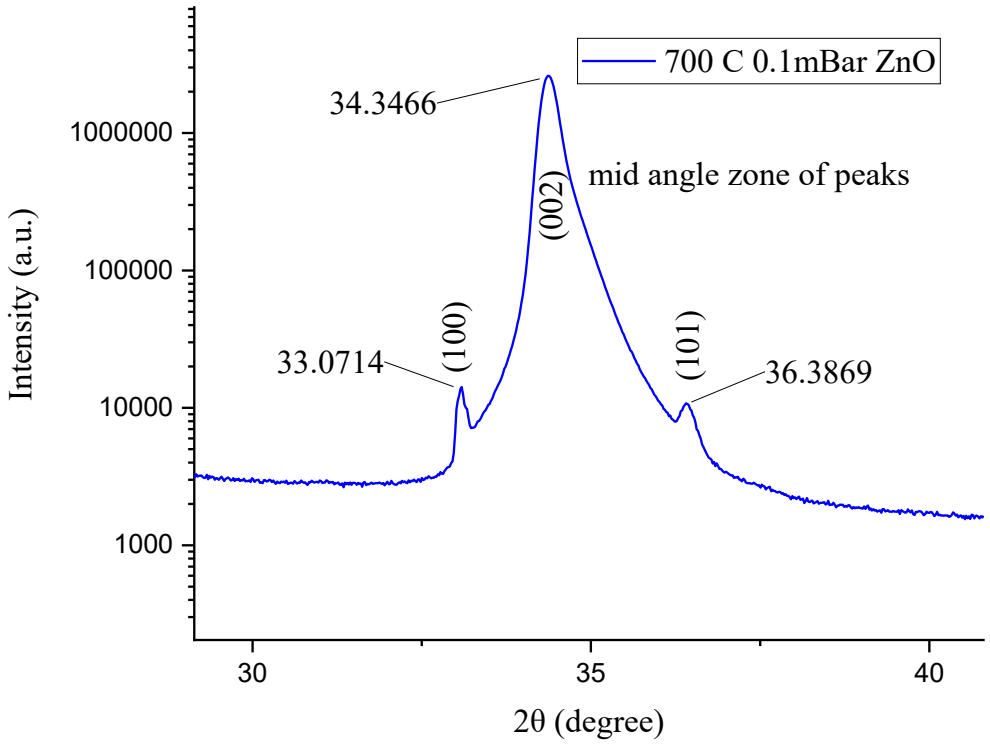

Figure 16: XRD peaks in mid 2θ range of sample#1 grown at 700 C

notice that a tiny shift (~0.3 degree) is noticeable in the substrate peaks in the ZnO sample. This

is normal as many literatures show that the original substrate can experience a strain and hence results in small shift in their XRD pattern when the thin film is grown on them. If the shift is in miniscule, it is acceptable as the original peak generated.

The figures represent XRD patterns of as grown ZnO thin films (figure 17-19). Multiple samples were grown using PLD method. Dominant peak of diffraction can be seen at 2θ = ~34.35° and this peak corresponds to wurtzite hexagonal phase of (002) and a also two extremely small diffraction peak can be seen at 2θ= ~33° and 36° and a medium strength peak can be seen at 72.56 which corresponding to the phase of (004). The crystallinity and its quality are understood using the full width half- maximum and the strength of ZnO (002) peak. A table-2

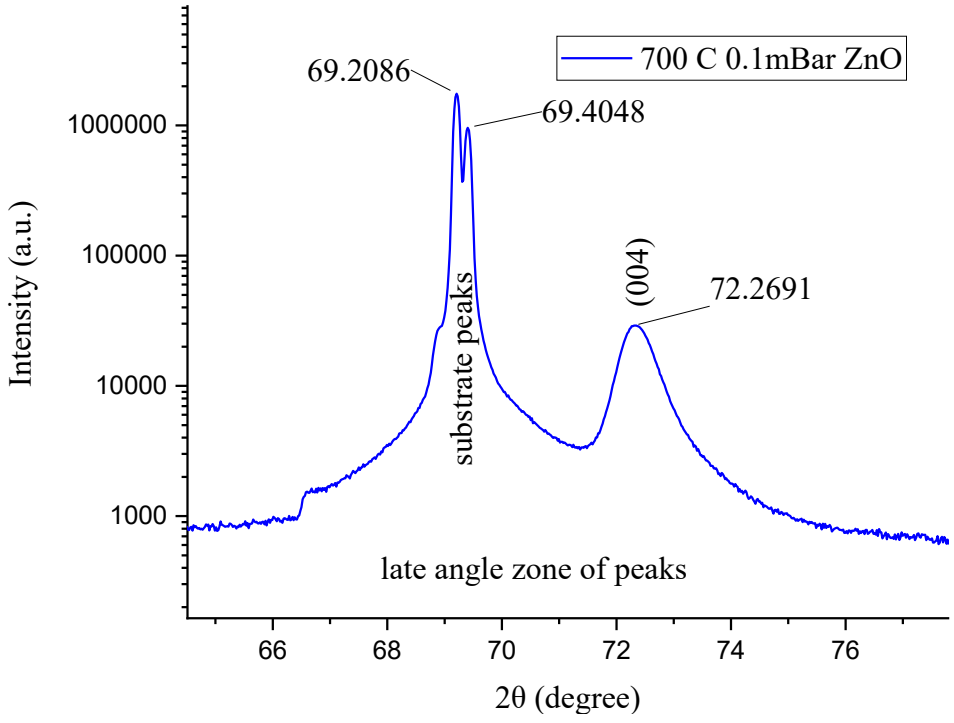

Figure 17:XRD peaks in late 2θ range of sample#1 grown at 700 C

represents the values for several phases of the 700C sample of the same film. Smaller value of

FWHM indicates better crystalline qualities of the synthesized film. It says that the crystalline size of PLD are larger than the usual as we used this PLD method. The proposed method applies the function of the peaks as were described by Gaussian function and calculated the half-width each of the peaks to be taken into consideration. Using a constant applicable for ZnO as K=0.9 is applied here with the wavelength of 0.15046 nm, and the θ is just the half of the plots 2θ. The

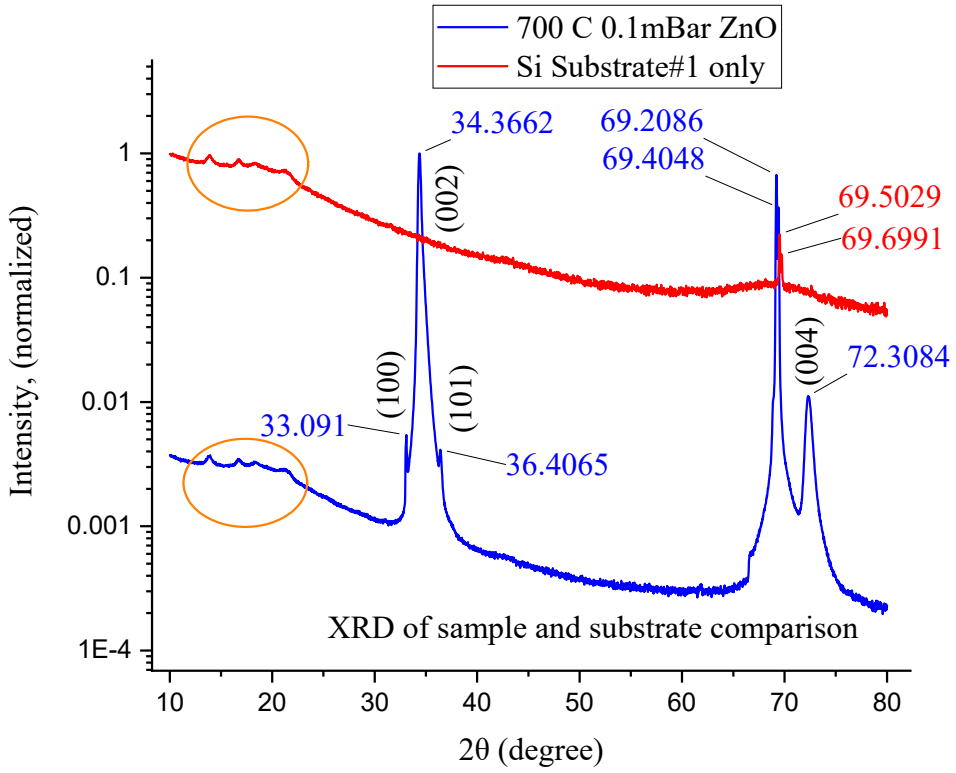

Figure 18: XRD of ZnO film grown on Si substrate#1 shown with the substrate XRD plot

FWHM values were obtained using the peak fitting analysis in Origin which resulted into the value of β in radian angle. The equation used is, $D_{\mathrm{hkl}} = \frac{\mathrm{K}\times\lambda}{\beta_{\mathrm{hkl}}\times\cos\theta}$. Debye-Scherrer formula can provide the crystallite size as given below. We can also calculate the crystal's lattice parameter using the XRD data available. As the peak from (002) plane gives us the h, k and l, and the

diffraction angle is obtained from the XRD, we can easily derive the lattice parameter a and c from the relationship of d, h, k, l, a &c with the angle of diffraction [22]. The lattice spacing of the ZnO film lattices for the mentioned parameters was calculated using the equation of Bragg's

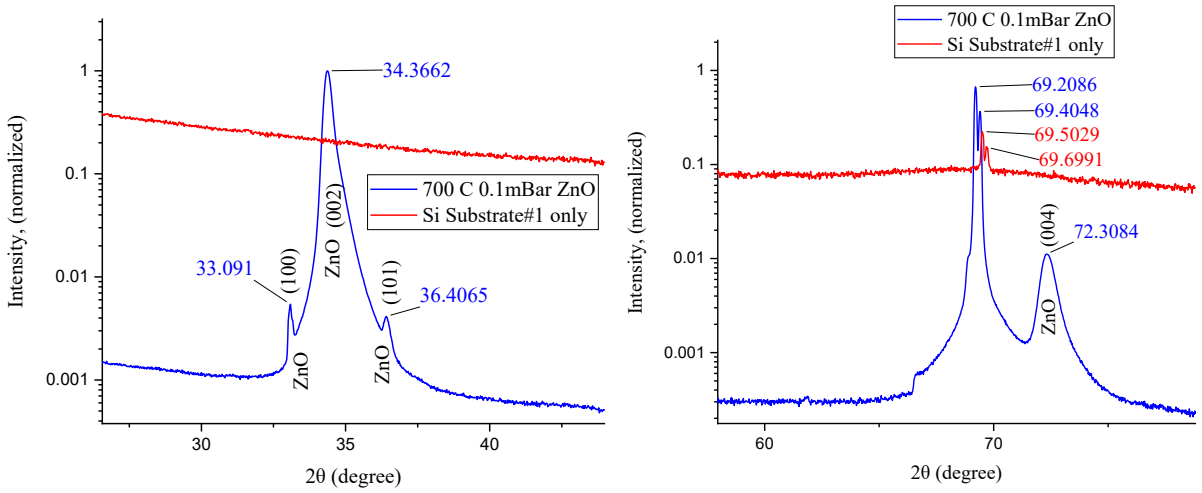

Figure 19: Regions of XRD plot of ZnO film on Si substrate#1 (shown with the substrate)

relation: d=λ/(2sinθ), here θ is the angle between normal to diffracting plane and incident X-ray, λ is the wavelength of X-rays, which is in the lab of PAMS, MSU was the x-ray radiation having wavelength 1.5406 Å. The lattice parameters have been calculated using the following expression for hexagonal system, $\frac{1}{d^2} = \frac{\frac{4}{3}\times(h^2+hk+k^2)}{a^2} + \frac{l^2}{c^2}$; using this relationship, the lattice parameters are calculated for this film and the following table-3 shows the values of the lattice parameters for this sample.

350°-500° C. As for the second sample, it is grown on a new substrate with lower resistance, but the preferred orientation is the same (100) Si p-type doped. This sample has a ZnO film grown at two temperatures, 350 and 500 C. There are studies on how an initial higher temperature like 500-700 would help build a better crystallinity in films in lower 300-350 C

instead of altogether lower 300-350 C of temperature. The initial higher temperature creates a

Table 2: Crystallite size of sample#1 grown at 700 C

Sample	K	Position	λ (nm)	FWHM	β (rad)	D (nm)	hkl
700° C	0.9	34.37°	0.15406	0.65282	0.011393	31.60	(002)
700° C	0.9	72.36°	0.15406	0.62877	0.010974	15.65	(004)

Table 3: Lattice parameters of sample#1 grown at 700 C

Sample	2θ	d_{hkl} (A)	hkl	a (A)	c (A)
700° C	34.35	1.37	(002)	3.16	5.15
450° C	34.59	1.357	(002)	3.13	5.11

better epitaxy for a subsequent lower temperature deposition on the substrate. This new substrate has a slightly different but mostly the same XRD peak response compared to the previous substrate, with a peak sharp at ~33 deg, another sharp peak pair at ~69 deg and two less salient peaks at ~67 and ~76 deg. The peak pair confirms the preferred orientation (100) of Si substrate and this plot would help distinguish the ZnO peaks from the redundant substrate peaks. Now if we compare figures (20-21) closely, the peaks those are not from the substrate but from the ZnO films are apparent. The (002) plane is showing its big spiked peak at ~34.50 and the (101) showing a less dominant peak at ~36.48 deg (figure-22). Again the (004) has a small spike at ~72.54 deg (figure-23). These data can determine the crystallite size using the same procedure as the previous sample (Debye-Scherrer method) and this calculation is shown below in the table-4.

Here, we can see that the FWHM is bigger for the (004) peak, and the size for (002) is

also smaller than the previous one and hence the crystallinity of film is less robust than we expected in a two layer of ZnO grown in two temperatures. Now as the previous sample, we can calculate the crystal's lattice parameter using the XRD data available. As the peak from (002) plane gives us the h, k and l, and the diffraction angle is obtained from the XRD, we can easily derive the lattice parameter using the equation of Bragg's relation: $d=\lambda/(2\sin\theta)$, here θ is the angle between normal to diffracting plane and incident X-ray, λ is the wavelength of X-rays, which is in the lab of PAMS, MSU was the x-ray radiation having wavelength 1.5406 Å.

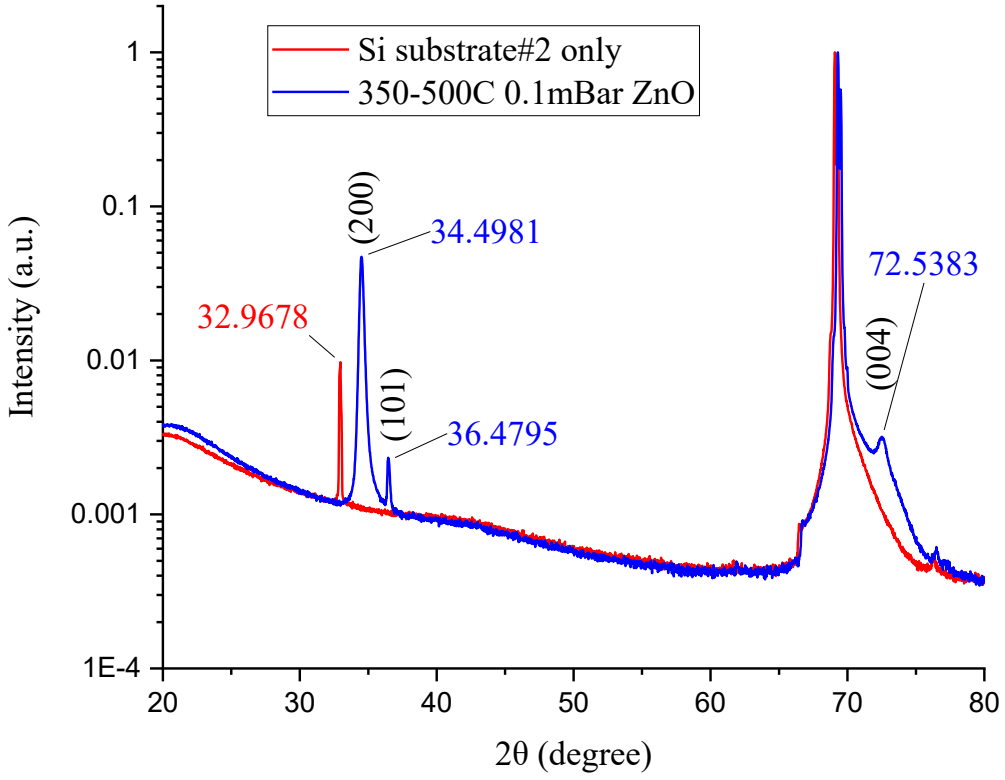

Figure 20: XRD plot of ZnO film (350 C) on the substrate is shown with the substrate

The lattice parameters have been calculated using the following expression for hexagonal system, $\frac{1}{d^2} = \frac{\frac{4}{3}\times(h^2+hk+k^2)}{a^2} + \frac{l^2}{c^2}$; using this relationship, the lattice parameters are calculated for

this film and the following table 5 and 6 shows the values of the calculations [22]. Only the dominant peak of (002) is calculated here.

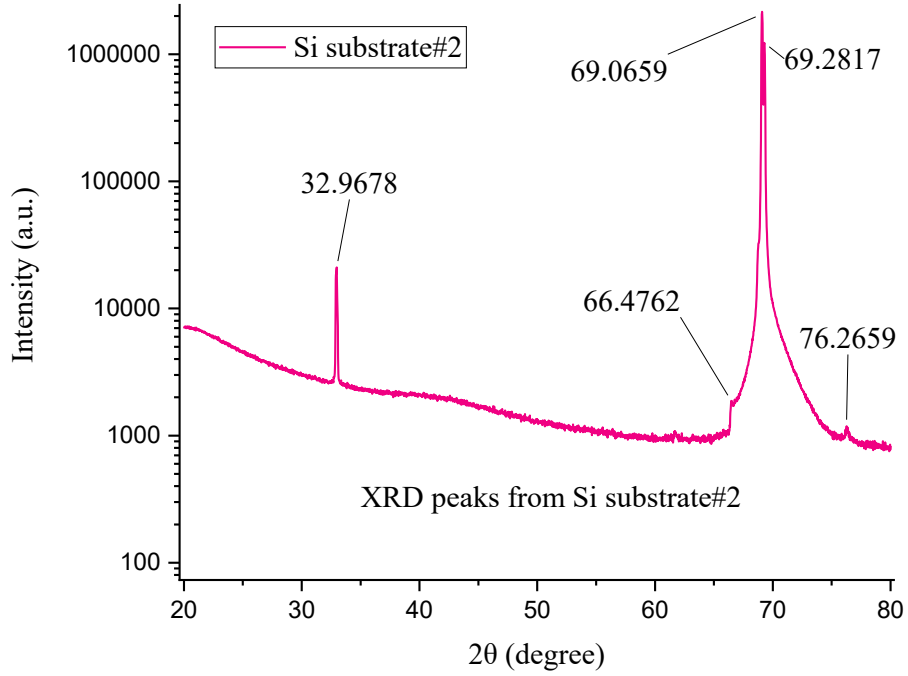

Figure 21: The XRD plot of substrate#2, Si (100) lower resistance

Table 4: Crystallite sizes for sample grown at 350-500 C

Sample	K	Position	λ (nm)	FWHM	β (rad)	D (nm)	hkl
350/500° C	0.9	34.5	0.15406	0.33881	0.00591	24.55	(002)
350/500° C	0.9	72.56°	0.15406	2.04923	0.03577	4.81	(004)

500 C. This sample is grown at 500 C on the second substrate. Now if we compare the XRD plot of the ZnO+substrate and the substrate, the peaks those are not from the substrate but from the ZnO films are apparent (figure-24). The (002) plane is showing its big spiked peak at ~34.57 degree (figure-25). Again the (004) has a small spike at ~72.54 deg (figure-26). The

plane of (101) shows almost no discernible peak in the plots and the (004) peak is also at ~1% of the magnitude of the (002) plane's peak. Hence at 500 C and in this substrate, the (002) is mostly dominant unlike the previous ones which has additional three mini planes present. We can use this data for determining the crystallite size using the same procedure as the previous sample (Debye-Scherrer method) and this calculation is shown below in the table-5.

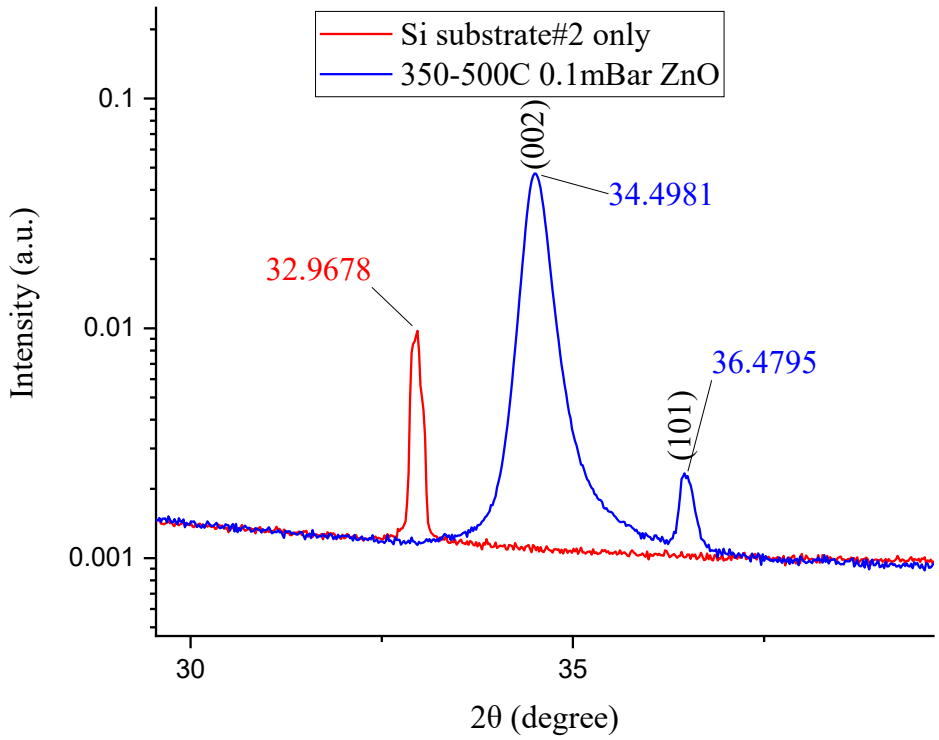

Figure 22: XRD plot o ZnO film (350 C) is shown with the substrate (mid region)

film. Now as the previous sample, we can calculate the crystal's lattice parameter using the XRD data available. As the peak from (002) plane gives us the h, k and l, and the diffraction angle is obtained from the XRD, we can easily derive the lattice parameters (table-6).

Here, we can see that the crystallite size is quite large for the (004) peak and the size for (002) is also significantly big which shows us a promising crystallinity and robustness of the thin

film.

500 C, 30 Mins Anneal. This includes an extra 30 mins anneal at 500 C after the growth which was not included in the last sample. The extra annealing changed the previous sample by a small degree.

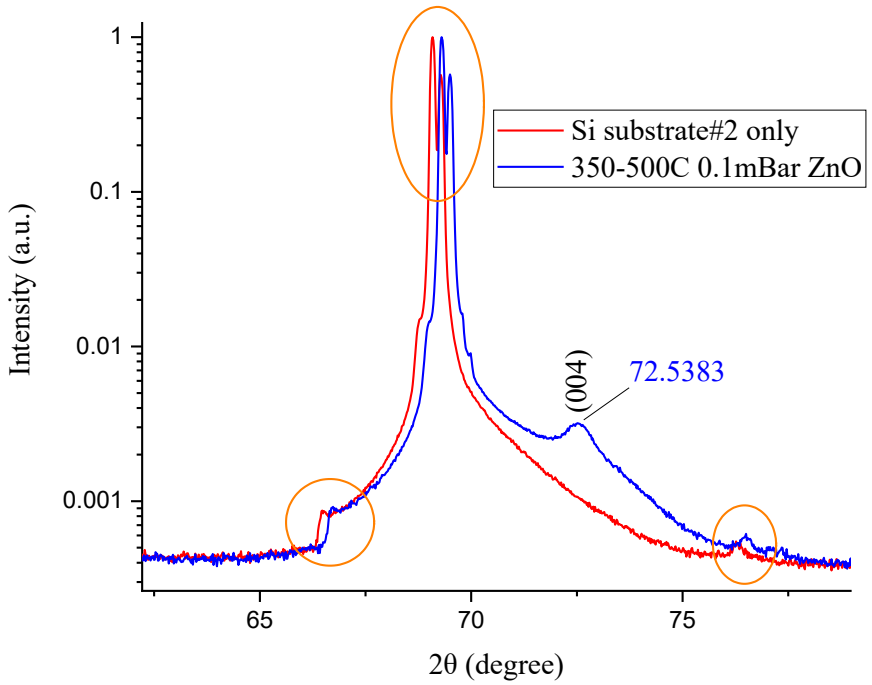

Figure 23: XRD plot o ZnO film (350 C) is shown with the substrate (late region)

Table 5: Crystallite size for sample grown at 500 C

Sample	K	Position	λ (nm)	FWHM	β (rad)	D (nm)	Hkl
500° C	0.9	34.58°	0.15406	0.26583	0.004640	31.29	(002)
500° C	0.9	72.62°	0.15406	0.56864	0.009925	17.34	(004)

The main peak at ~34.44 (figure-27), a little shifted backwards, and the peak is reduced a lot in magnitude as well. On the other hand, the (004) peak (figure-28) also became blunt

compared to other samples. Surprisingly, the annealing created two ridiculously small spike to be more visible than the rest of the samples. Nevertheless, these two spikes are negligible compared to the other large spikes. Hence the annealing reduces the spikes of the major peaks and creates two extremely small spikes. Overall, the (002) plane dominates by a large scale.

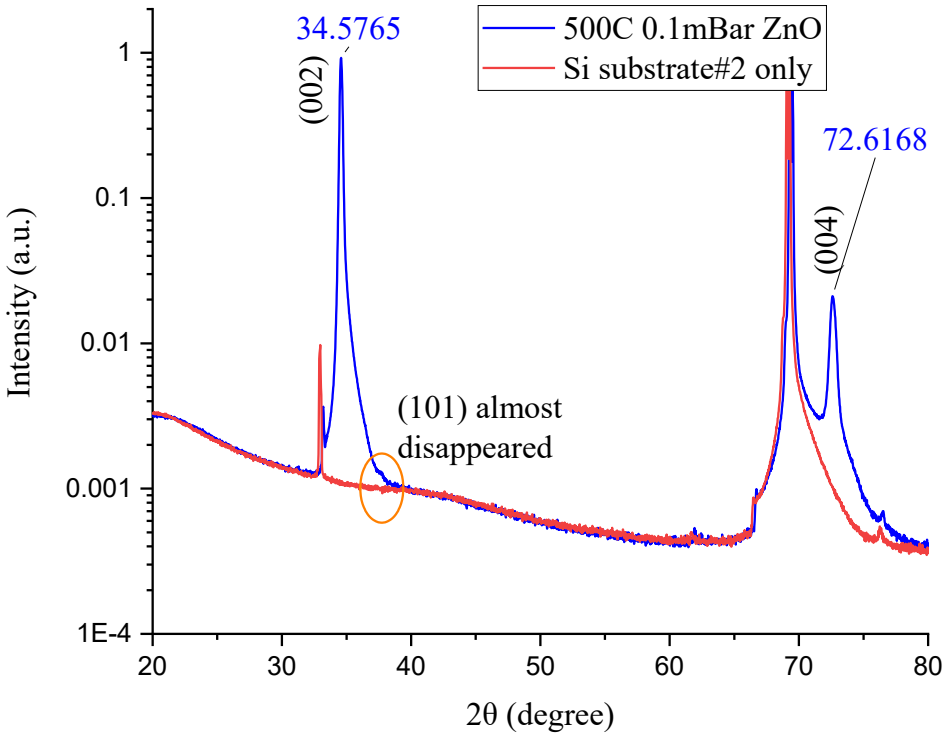

Figure 24: XRD plot of ZnO film (500 C) is shown with the substrate

We can use this data for determining the crystallite size using the same procedure as the previous sample (Debye-Scherrer method) and this calculation is shown below in the table-7 here. The table-7 shows that the crystallite size of the (002) preferential plane in ZnO film has somewhat same/reduced than the previous but the (004) direction suffered a huge reduction in

the crystallite size. This is expected as we saw a decrease in the peak intensity of the peak of the (004) plane in XRD analysis. Now as the previous samples, we can calculate the crystal's lattice

Table 6: Lattice parameter for sample grown at 350 and 500 C

Sample	2θ	d_{hkl} (A)	hkl	a (A)	c (A)
500° C	34.58	1.358	(002)	3.136	5.11
350/500° C	34.50	1.36	(002)	3.14	5.12

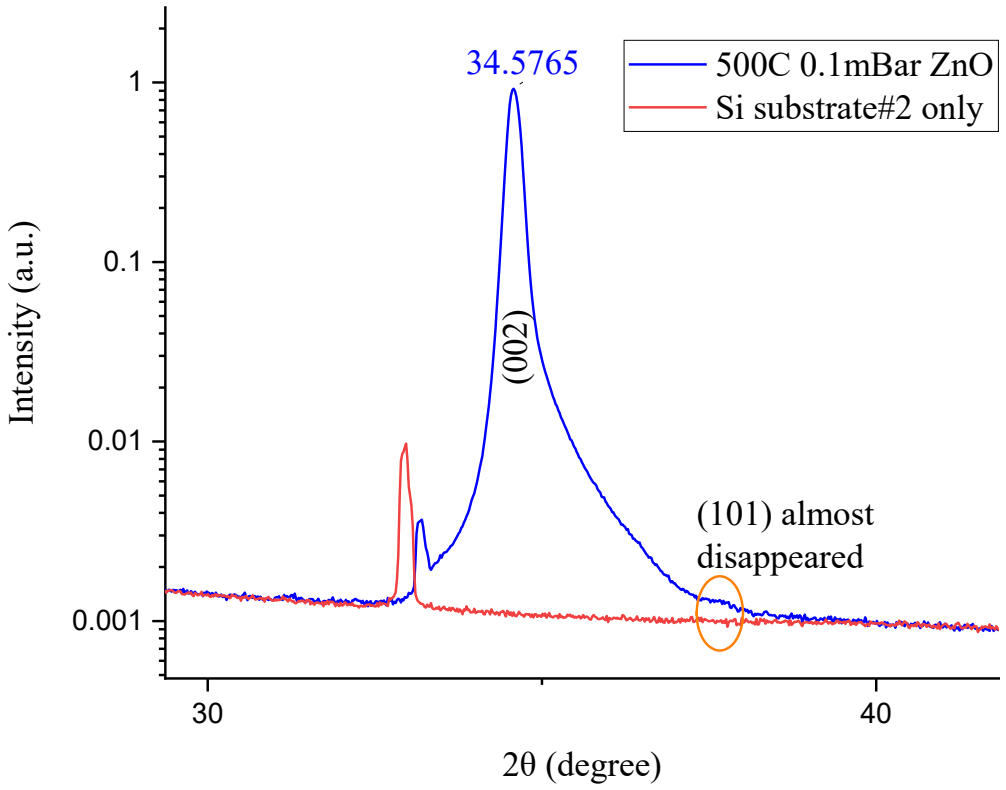

Figure 25: XRD plot o ZnO film (500 C) is shown with the substrate (magnified)

parameter using the XRD data (table-8). As the peak from (002) plane gives us the h, k and l, and the diffraction angle is obtained from the XRD, we can easily derive the lattice parameters.

Comparative Lattice Parameter and Crystallite Sizes. As from the XRD plots (figure-29), the x-ray diffraction angle was varying with the substrate and the temperature. The two

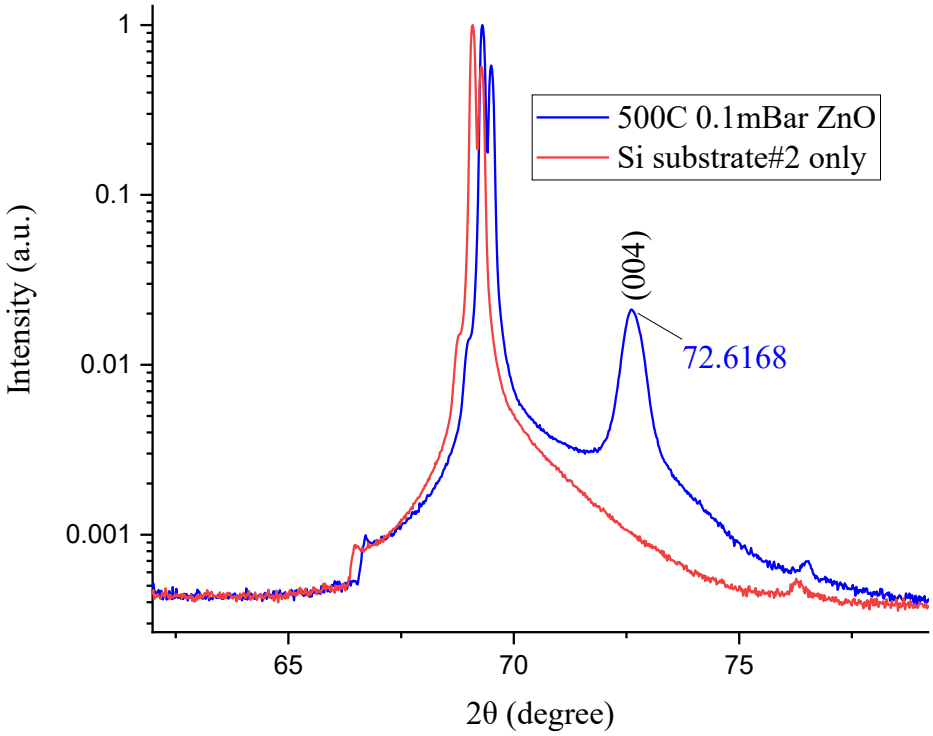

Figure 26: XRD plot o ZnO film (500 C) is shown with the substrate (magnified)

temperature of 450 C and 500 C without anneal seemed to have the close diffraction angle and

Table 7: Crystallite size of the sample grown at 500 C and annealed 30 minutes

Sample	K	Position	λ (nm)	FWHM	β (rad)	D (nm)	hkl
500° C	0.9	34.44°	0.15406	0.36588	0.00639	22.73	(002)
30 min anneal	0.9	72.50°	0.15406	18.4669	0.3223	0.53	(004)

annealing shifted the angle backwards. As a result, the lattice constant also increases as the

annealing happened. The higher temperature (700 C) also reduces the diffraction angle and hence increases the lattice constant. The crystallite sizes of the film also depend on the parameter of the growth and it also shows the relevance with the other properties of the thin films, i.e. the

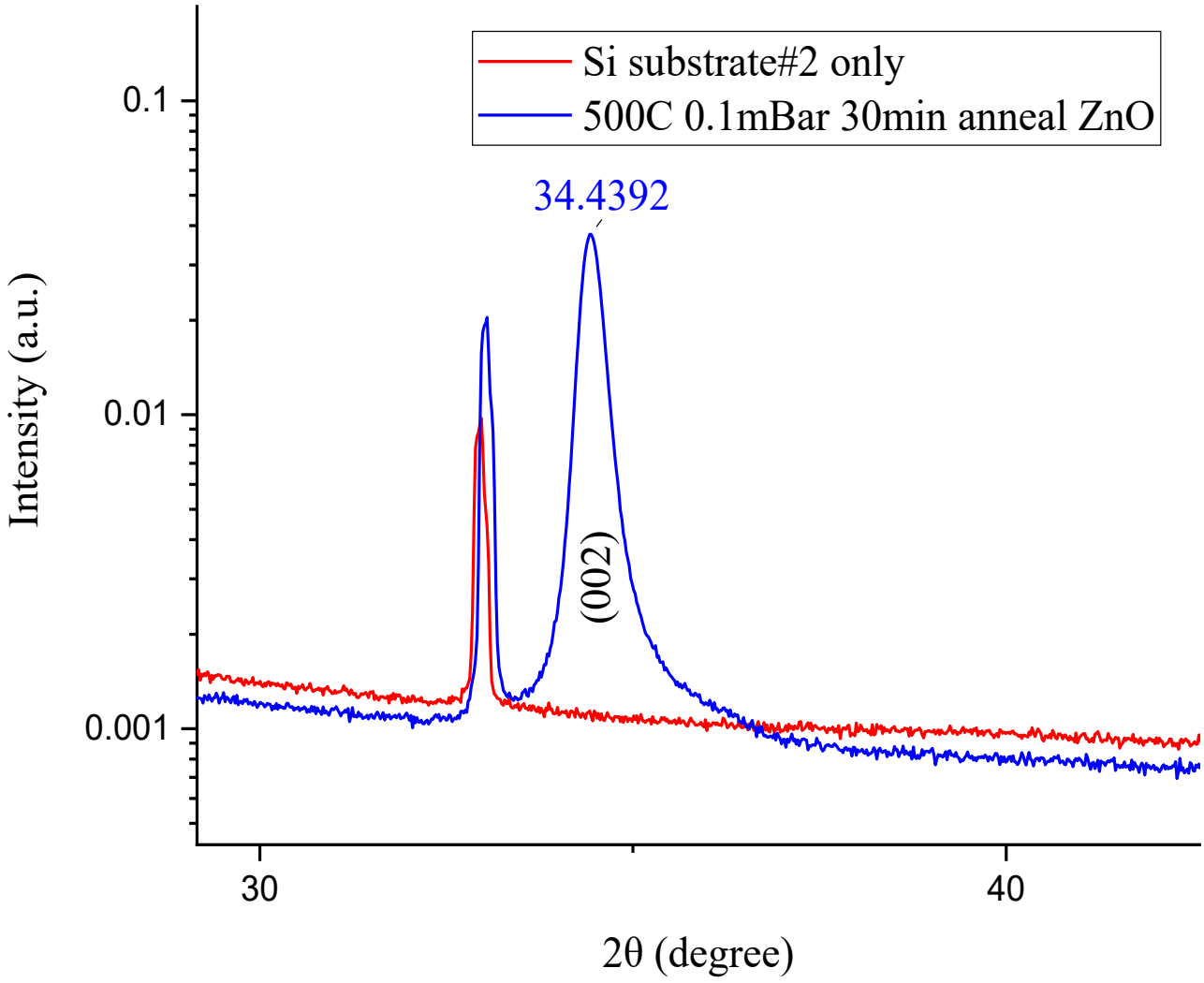

Figure 27: XRD plot o ZnO film (annealed 500 C) is shown with the substrate

photoluminescence and the FET performances. We can see the biggest size of crystallite is possessed by the 700 C sample which seems to be the best performer in the FET properties. Accordingly, the next best performer is the 500 C sample of the next substrate and it has the

Table 8: Lattice parameter of the sample grown at 500 C and annealed 30 minutes

Sample	2θ	d_{hkl} (A)	hkl	a (A)	c (A)
500° C, annealed	34.44	0.1363	(002)	3.147	5.1298
500° C	34.58	1.358	(002)	3.136	5.11

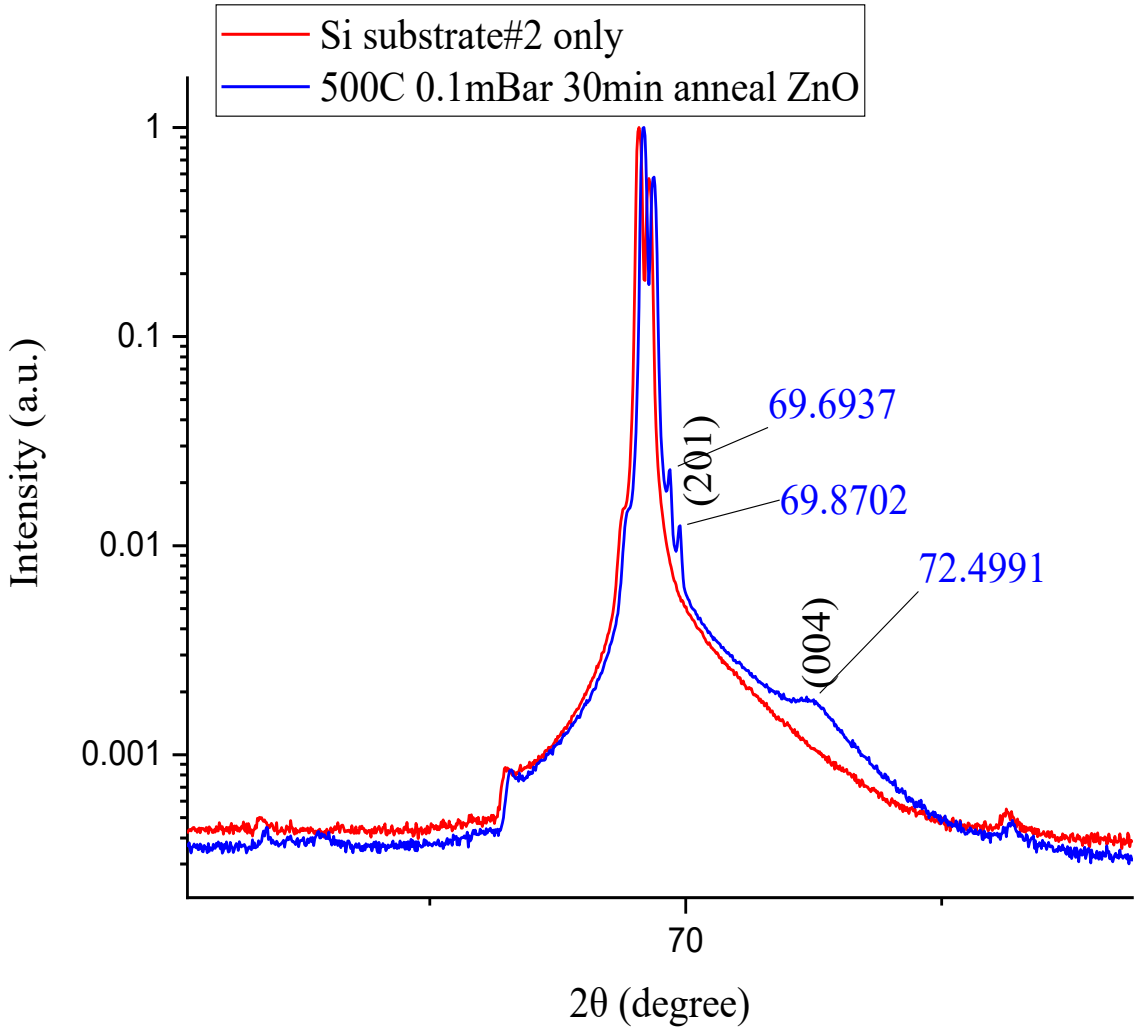

Figure 28: XRD plot o ZnO film (annealed 500 C) is shown with the substrate (magnified)

almost same size whereas the other two samples performed worse in the PL and the crystallite size is also smaller in comparison (figure-30,31, and 32).

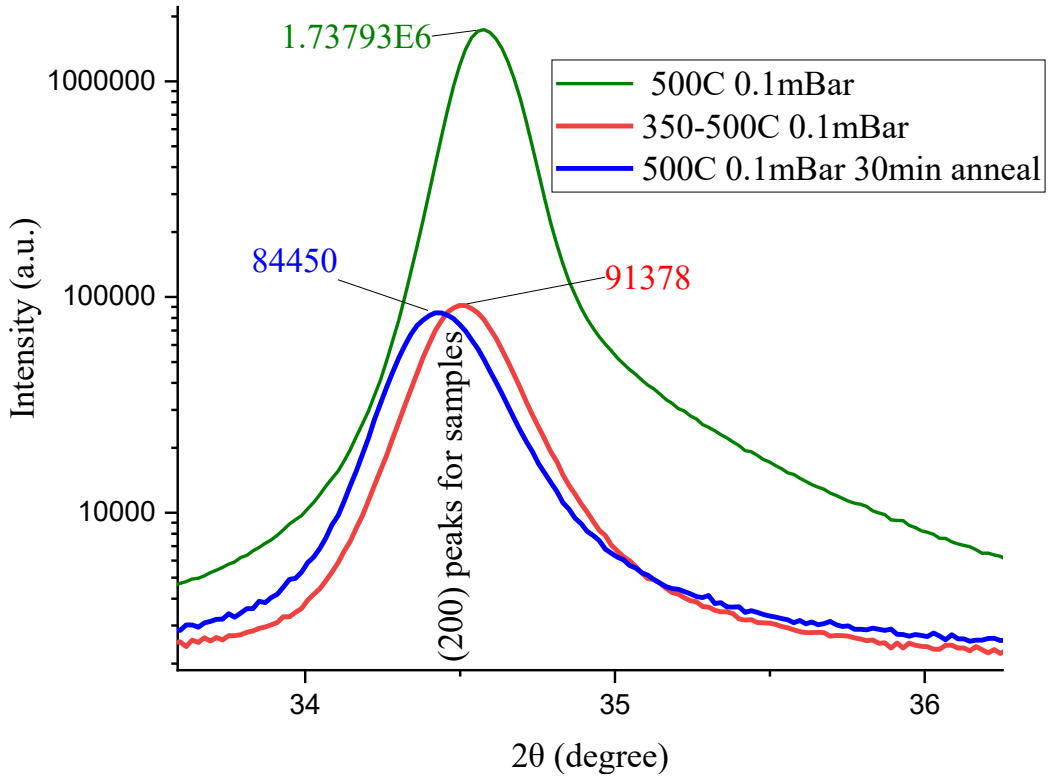

Figure 29: Relative intensity of X-ray diffraction peak (002) of ZnO sample

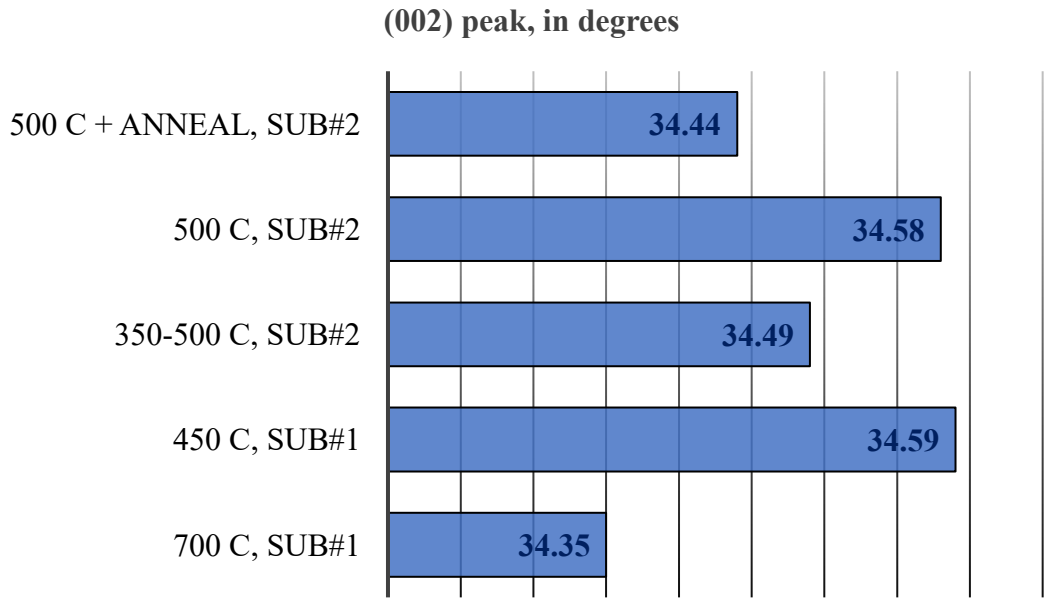

Figure 30: Peak of the (002) peak in different samples

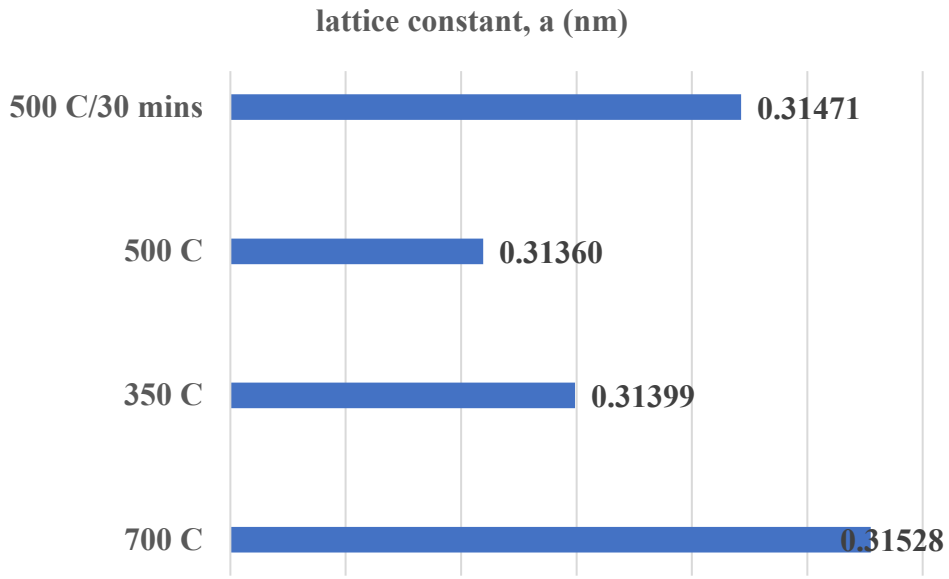

Figure 31: Lattice constant for different samples

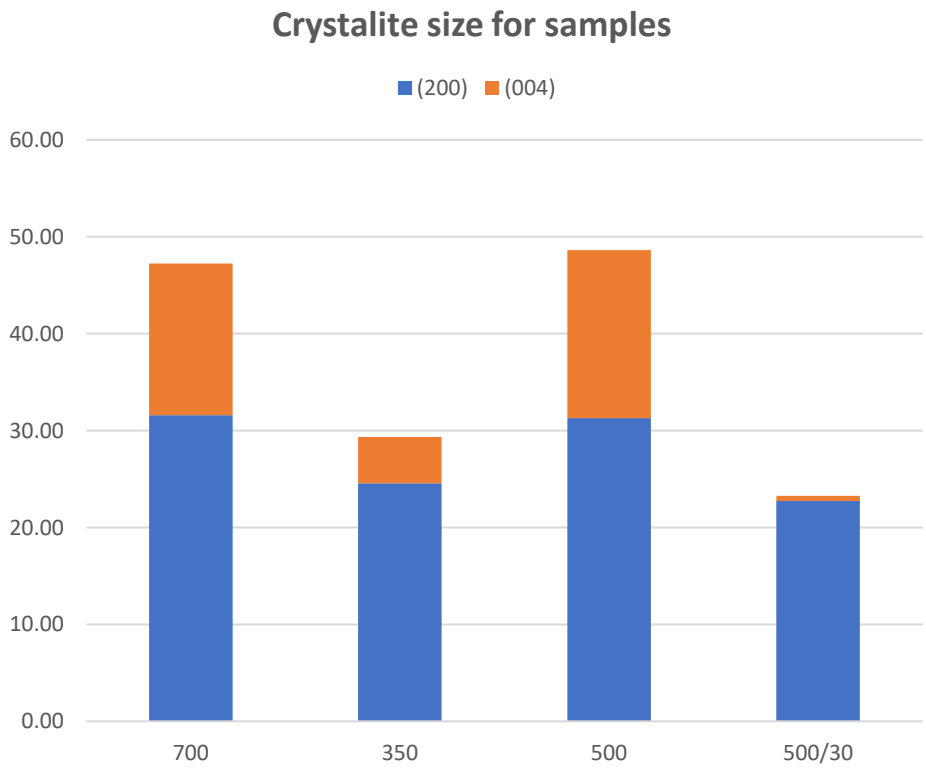

Figure 32: Crystallite sizes of the samples

Photoluminescence (PL)

The films of different growth parameters are tested for the photoluminescence property (figure-33,34) for a correlation between the FET performance and also the XRD analysis, crystallite size and lattice parameters. It is convenient to divide the PL spectra (table-9) along the frequency to understand the behavior and significance of the peaks and spikes. We have UV

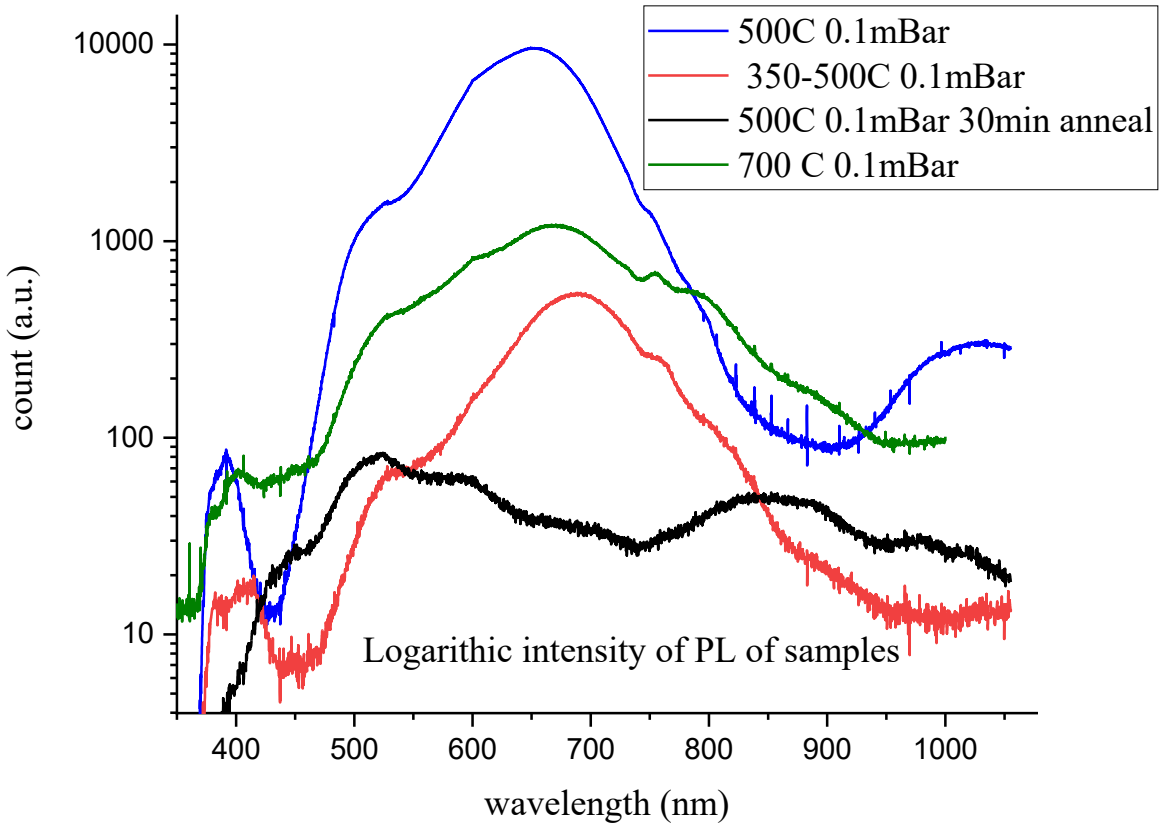

Figure 33: Logarithmic plot of photoluminescence of the samples on substrate#2

regions, along with a broad visible region consisting with the green, yellow and orange, blue and red zones as the most prominent divisions. Each zone will have their own significance as described later. The most inherent PL spectrum for ZnO is the UV zone which gives a

characteristic nature and it is due to the combination of the excitons and characteristic transition at the edge of bands [23].

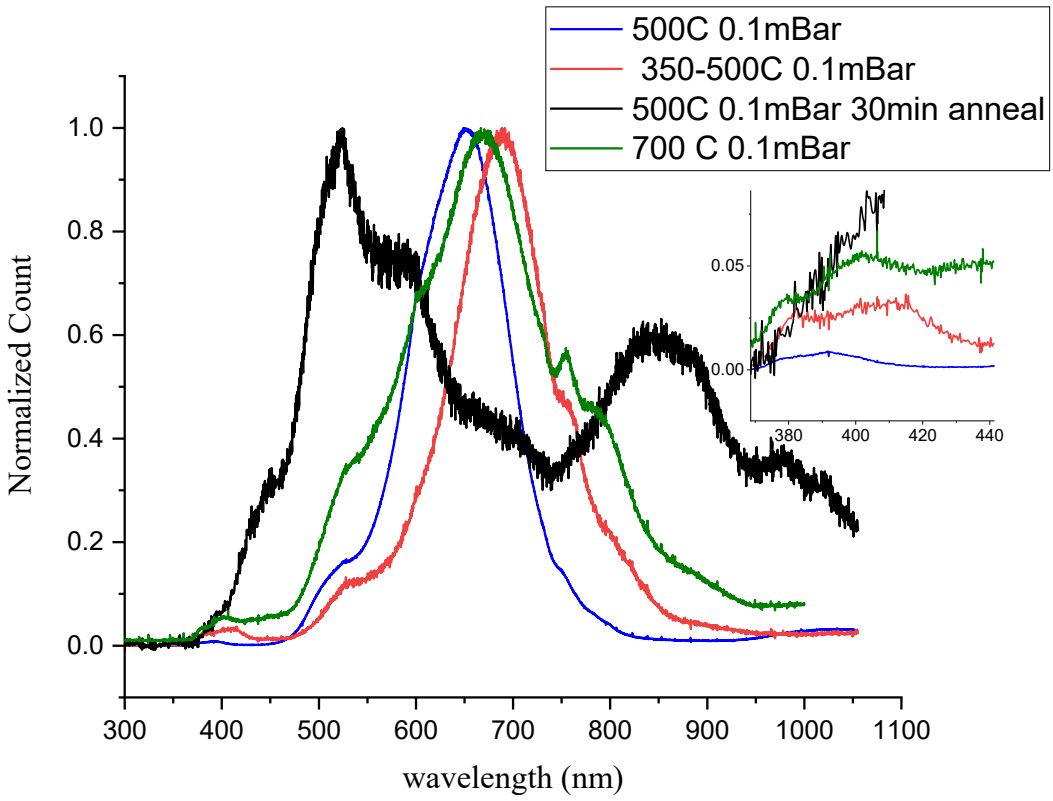

Figure 34: Linear normalized plot of PL for all the samples

These figures-33,34 will help us understanding the PL characterization patterns for the samples. The figure-33 here shows the effect of annealing where the annealed sample possesses some unique emission peak feature comparing to the similar other two samples on the same substrate. Again, the figure-34 shows similarity of the PL emission peaks of the 700 C sample on the different substrate and apparently the temperature made the probable intensity as the 500 C on the second substrate shows the most prominent PL emission considering ZnO thin film as count intensity considered. The comparative emission peaks are discussed segment by segment

in the next parts.

The deconvoluted peaks figure-35,36,37,38 are the best method to analyze the peak emission in different regions. The samples are analyzed as the deconvoluted peaks are arranged side by side for better understanding. This will give us the opportunity to compare the substrate effect and the temperature effect on the photoluminescence of the thin film samples.

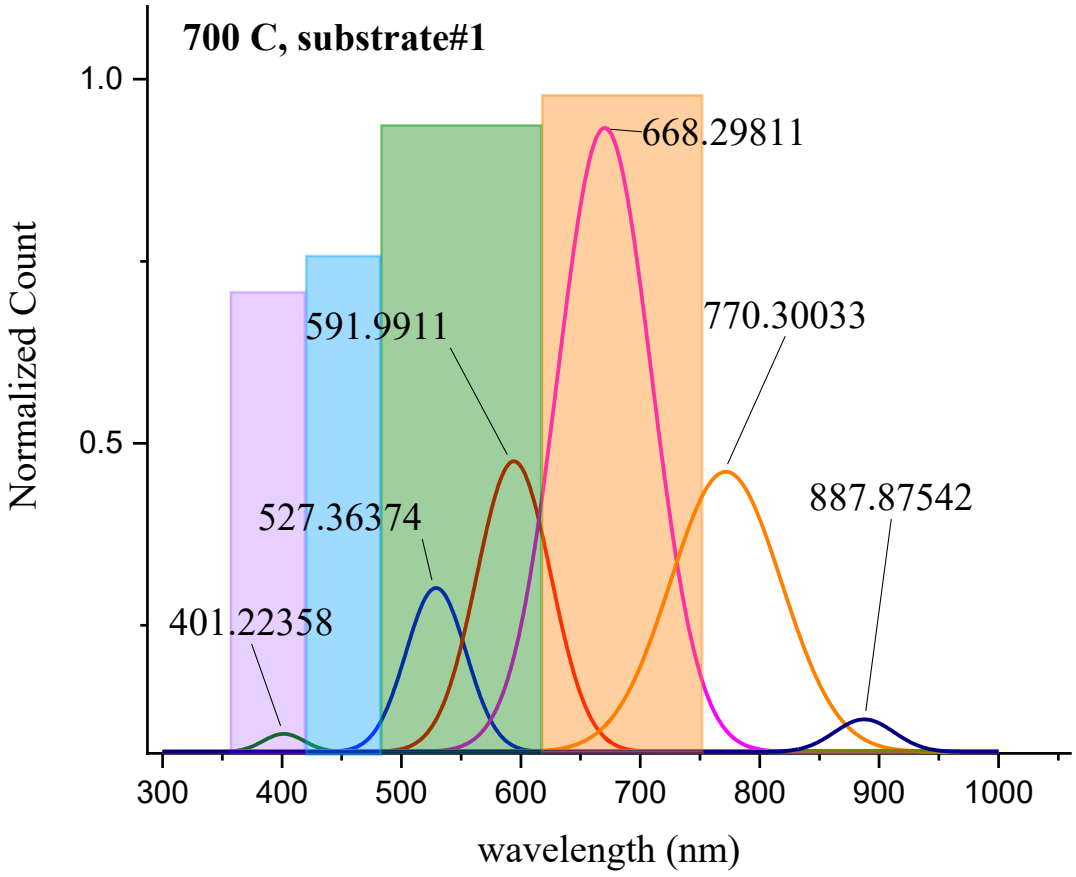

Figure 35: Deconvoluted peaks for samples of 700 C in different emission zones

Figure 35, 36, 37, and 38 show the logarithmic intensity along the wavelength in near UV region and the UV peak is strongest for the 500 C growth (at 391 nm) sample compared to its annealed and the 350/500 C peak. The annealed sample has almost no UV peak compared to the

other samples. This means the 500 C sample has the highest exciton binding tendency as a great ZnO sample should and thereby making it a great ZnO thin film candidate for an FET. The annealed sample was annealed at 500 C in oxygen environment making it have less oxygen deficient in the lattice which obviously displays in its absent UV PL peak. Again, when the 700 C sample is examined, we can observe the UV peak at 401 nm like the unannealed samples.

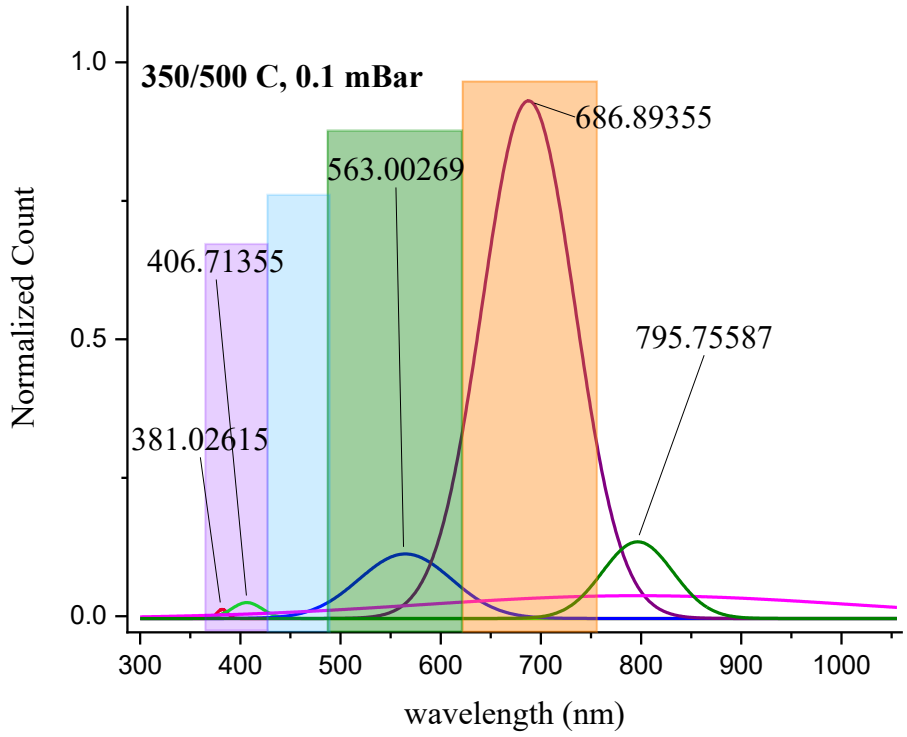

Figure 36: Deconvoluted peaks for samples of 350 C in different emission zones

In the green region we have one very dominant peak in the annealed 500 C sample of ZnO while the other two has one blunt peak each in their PL intensity. The figure showing the green zone has a normalized linear scale of PL intensity showing the spikes present in the PL plot for the samples. This is a defect emission peak which can be caused by numerous reasons like, the vacancy of oxygen or zinc, interstitial atoms, misplaced atoms of oxygen in zinc's stead or vice

versa etc. As we know that the zinc vacancy formation energy (5.4 eV) is larger than the oxygen vacancy formation energy (3 eV), the probable defect is mostly due to the either the interstitial oxygen or the oxygen vacancy [24]. This means the interstitial oxygen might be implanted in the lattice while annealing, and this instead of the vacancy is responsible for this.

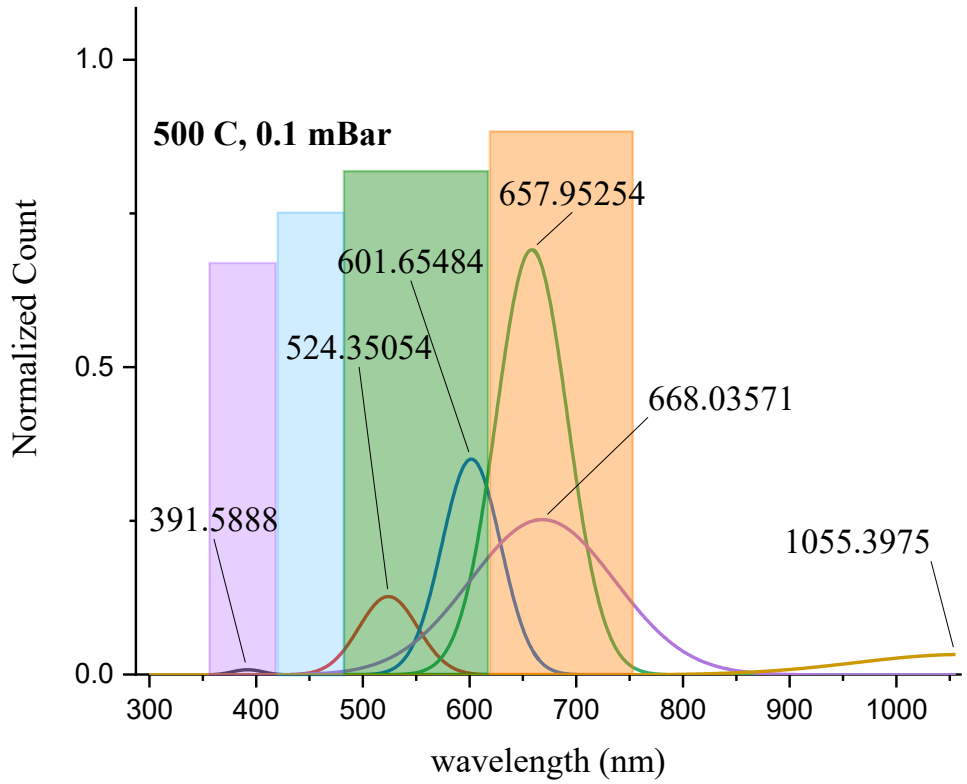

Figure 37: Deconvoluted peaks for samples of 500 C in different emission zones

emission peak in PL of the ZnO film samples. The defect emission in green zone is similar for the 700 C sample as the unannealed sample as it gives a peak at 522 nm. The figure-38 shows the normalized linear PL counts in orange zone for the three samples, and we can see that except the annealed film, the other two samples contain the orange peak in their PL plot.

The orange peak denotes the oxygen vacancy and the zinc interstitial atoms in the sample

[25]. The orange peak in present in non-annealed sample and annealing in oxygen removes/reduces the defect peak. This means the non-annealed films has dominantly oxygen vacancy and probably the zinc interstitial atoms are low in number. The reason is the defects reduce the near band electronic recombination and thus the annealed film experiences the absence of the peak in orange zone. As the other zones the 700 C gives a similar peak at 668 nm in the orange region as the non-annealed samples do.

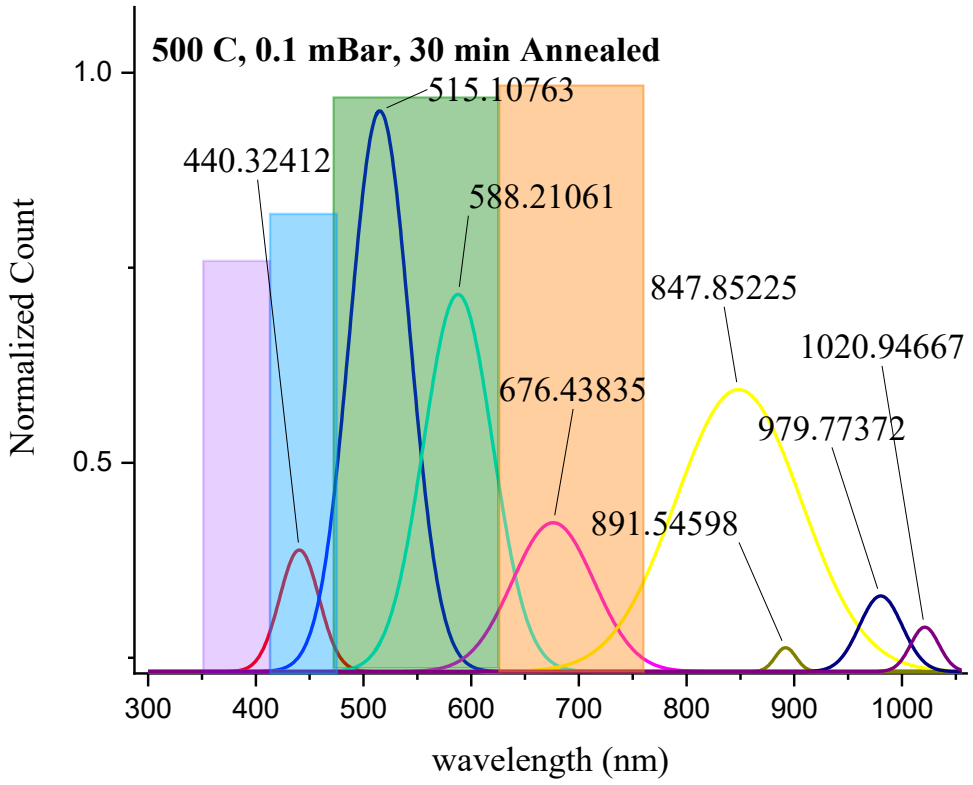

Figure 38: Deconvoluted peaks for samples of 500 C annealed in different emission zones

Figure 38 shows the blue emission in the normalized linear PL spectrum, and this shows that the annealed ZnO film has a blue emission peak but the other three does not have one. The blue emission is caused by the electronic transition of interstitial donor level to the acceptor

level. This transition is the result of Zn vacancies in the films [25]. As we annealed the ZnO film, it probably caused the oxygen abundance which might on the other hand caused some Zn deficiency which is responsible for the blue emission peak of the film. The Zn vacancy is a function of the square root of the oxygen pressure and thus the high oxygen pressure of annealing (0.1 mBar) could be a reason for the blue defect peak in the PL plot of the annealed sample. It also not surprising that the 700 C sample's PL peaks are devoid of the peak in this region just like the other non-annealed samples do.

Finally, in order to understand the quality of the ZnO film, the comparative original PL intensity is also a metric of the quality of the films where we can determine the overall quality of the film as an insulator layer for the FET device. This figure-39 has shown the

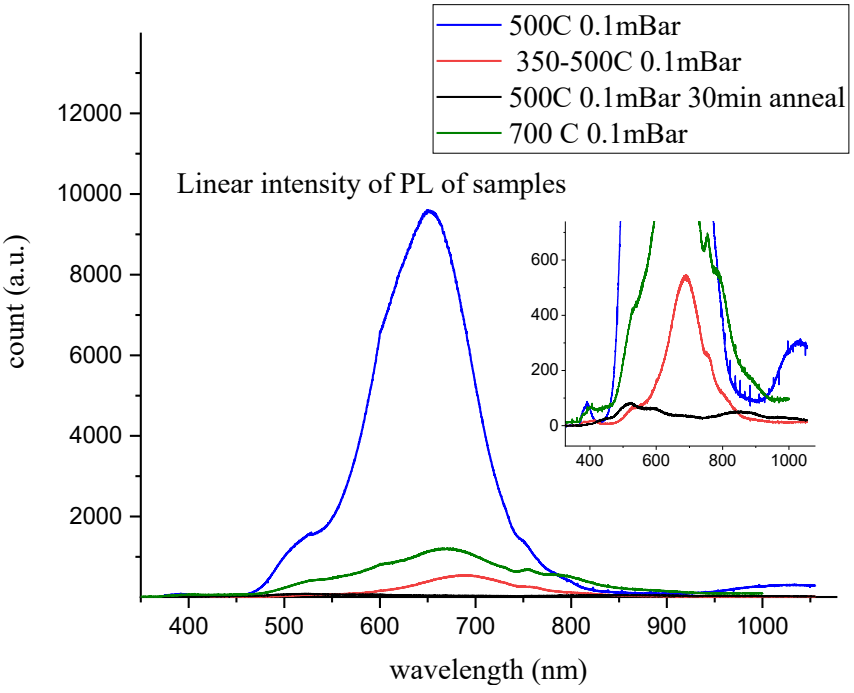

Figure 39: Linear intensity of PL peaks for samples in comparison

photoluminescence in the logarithmic scale against the wavelengths for the three samples. This is

evident that the 500C sample has a very high response in the PL, and the annealed and the lower temperature sample shows poorer peak response in PL. Hence the PL method conclusively demonstrates the 500 C grown sample as a superior one in crystallinity and structure.

Table 9: PL zones in a summary

	Near UV, 390 nm	Green, 540 nm	Orange, 650 nm	Blue 450 nm
700 C	strong	present	present	absent
350-500 C	present	present	present	absent
500 C	strong	present	present	absent
500 C -anneal	absent	strong	weak	present

Raman and Scanning Electron Microscopy

Figure 40 shows the generic nature of the Raman spectrum and figure-41 shows an SEM image of the ZnO films grown on the substrate. Since the doping of the film was not present, and the substrate material is chemically the same, the spectrum and the peak patterns are basically the same with some minor shifts.

Hence details of the Raman analysis have not been presented here. The spectrum of the 500 C sample is discussed here briefly as a representative one. There are two main Raman peak those are visible as the ZnO film renders, one is at around ~441 cm^{-1} and another is at around ~572 cm^{-1} region. There are also some broad non-salient zones around ~220-300 cm^{-1}. The peak at 441 cm^{-1} represents the E2 mode of ZnO film. The other peak at 572 cm^{-1} denotes the E1 mode of the ZnO film. There are also some other peaks, especially the very dominant and sharp peak at ~520 cm^{-1} which is from the Si (100) substrate. There are also some fewer dominant peaks from

the substrate at around 320 cm^{-1}. The ZnO peaks are mainly coming from

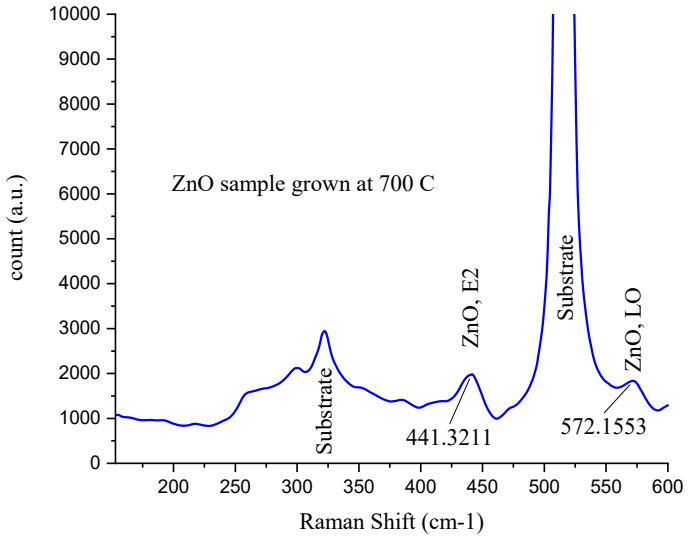

Figure 40: Raman spectrum analysis of the ZnO sample grown at 700 C

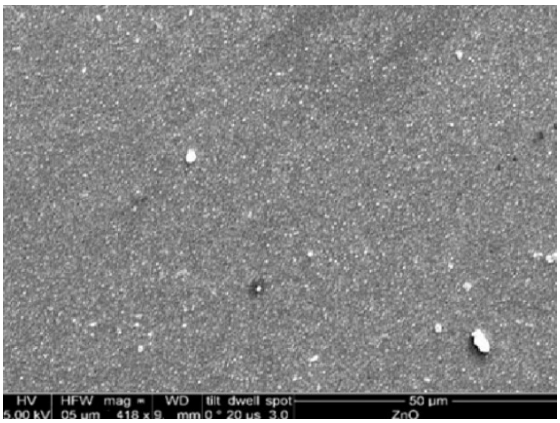

Figure 41: Scanning electron microscopic image of the sample grown at 500 C

the oxygen deficiency which the grown samples have, and they are more clearly understood using photoluminescence method in study. The Raman peaks due to this property is more dominantly visible when the temperature is very high to very low which is not in this study where we used moderate 350-700 C temperature.

The structure and physical morphology are a strong function of the temperature and the pressure of the growth [26]. As the temperature is varied the surface film morphology will change. Very low temperature (below 150 C) usually results in a very rough surface of the film [26]. The samples here are grown over 300 C and to 700 C which is conducive to create a smooth surface compared to the very low temperature surfaces. The SEM images could be zoomed well around 50 μm scale which apparently showed us a uniform surface without any big discontinuity and holes. This is promising for the suitability of fabrication of thin film transistors using these films. Figure 41 shows a film grown at 700 C as a representative of the samples as all the samples gave similar results in SEM imaging that is all the samples had fairly similar and smooth film without visible defect in the surface. Hence, the detailed study of comparative SEM image analysis is not made here in the thesis.

TFT (Thin Film Transistor) Characterization

The substrate here used is the high resistive silicon wafer cleaned and dried. The FET is made by the process mentioned, and the testing procedure is described in earlier sections. The electrical characterization involves the measurement of current from drain to source while varying the voltages applied through gate and source. To understand the electrical merit of the TFT, we have two relationships to use, one is the transfer plot and the other is the output plot. The output plot is the straightforward ohmic relationship between the two terminals of drain and source at various gate voltages applied. On the other hand, the transfer curve can be obtained as the current between the drain and source changes with the gate voltage at different drain-source voltages applied.

The ZnO slab/layer used here for FET fabrication is obviously of n-type, and hence it

creates the generic of an enhancement type field effect transistor. Hence the properties should closely resemble the nature and the relationships of that of mentioned above. The relationships those are found experimental is not too far from ideal for some cases.

Parameter#1 T=700C, P=0.1mBar, Substrate#1. To understand them the first FET batch is studied as shown here. The first batch of FET has the layer of ZnO grown in 700 C with the oxygen pressure of 0.1 mBar and no annealing was involved. Three cases of V_{DS} is created with a swing of $V_{GS,}$ and the drain to source current is observed in the Keithley micro current meter. As the table-10 and the figures 42,43 show, the FET had a steady current for an applied

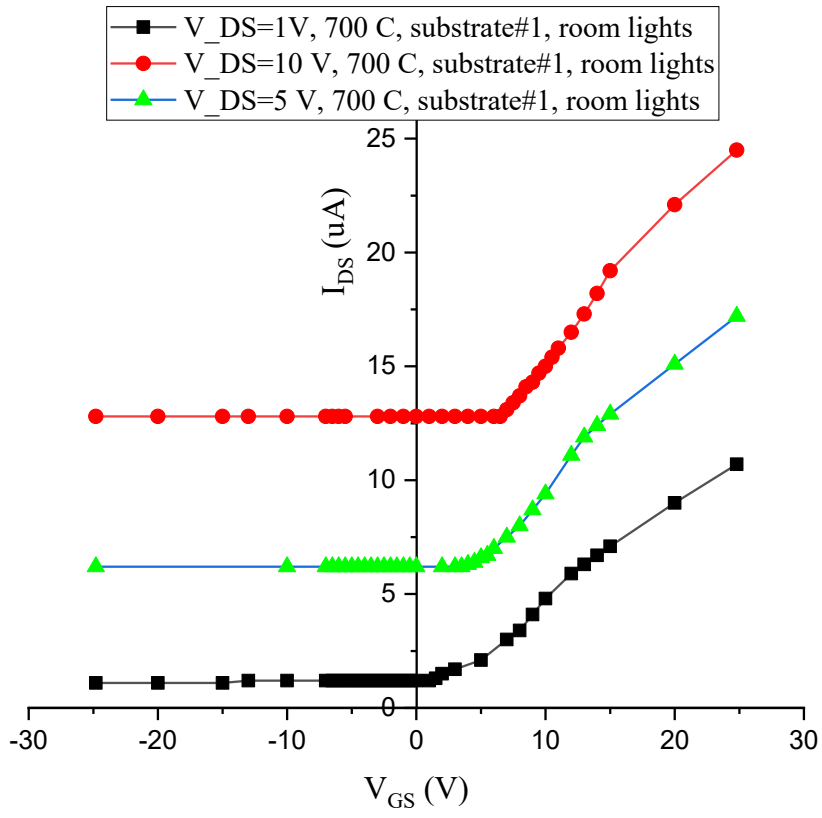

Figure 42: I_{DS}-V_{GS} of 700 C sample for different channel voltage in room light (μA Vs Volt)

drain to source potential difference. This current can be considered as an off-current and as the

graph, the amount of this current is in order of tens of mA and completely dependent on the applied D-S voltage in linear fashion. The current does not get a spike till the gate voltage reaches a certain value after which the current increases linearly. Here the electrons are generated by positive voltages between gate and source, and this agrees with the fact that the original channel layer is

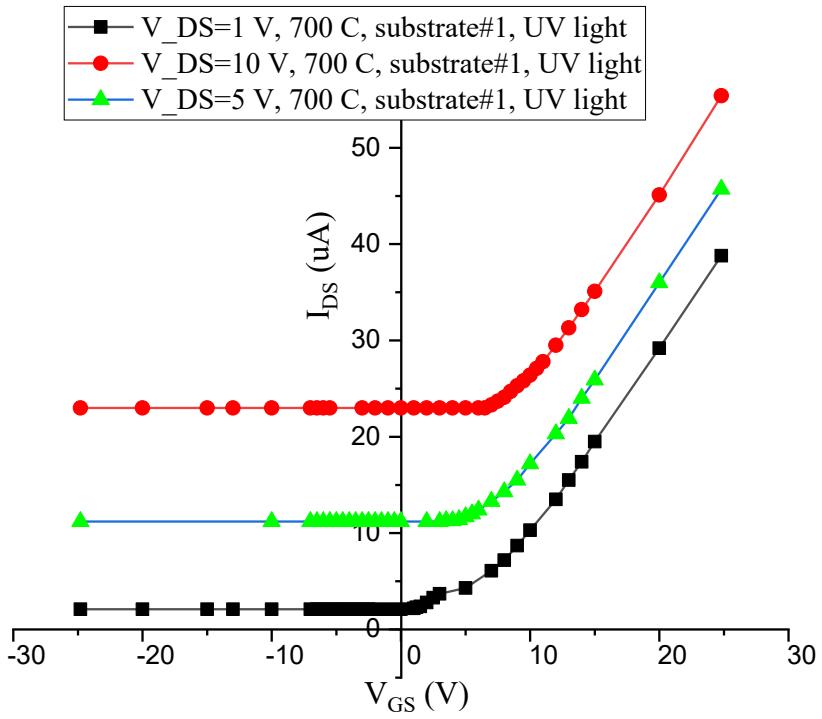

Figure 43: I_{DS}-V_{GS} of 700 C sample for different channel voltage in UV light (µA Vs Volt)

n-type. Some recent studies reported that the drain-source current reaches to saturation at around 35-40V at the gate, and the ohmic region to the saturation when the gate voltage is close to or above 35 V for laboratory scale ZnO TFT [19].

In this study the voltages applied to the gate was not above the 25 V mark, and any high voltage in a sustained manner would burn the sample and make the layer unstable due to the

thermal instability. Therefore, it is not observable in this FET that the saturation is not achieved in the operating ranges here for 700 C especially at UV lighted samples. Although the samples when not enlightened show a small curved nature in I-V as expected.

Table 10: On voltage required at the gate for 700 C sample in different light exposition

V_{GS} to switch on	UV light applied	UV light not applied
V_{DS}= 1 V	1.35 V	1.27 V
V_{DS}= 5 V	5.31 V	4.30 V
V_{DS}= 10 V	6.70 V	6.55 V

The cases of UV illuminated FETs show the on voltage higher than the cases with no extra light other than the room lights. Moreover, the applied gate voltage needed to switch on the FET device changes with the drain-source voltages, and here it is tested for 1, 5 and 10 volts applied between the terminals. So as the table-10 generated from the graph shows, as the drain-source voltage was increased, the gate voltage to switch on the device also increased.

The relationship of I-V through the drain-source is found mostly ohmic when the voltage at gate was applied within a 25 V range (figure-44), but the slope and the resistance did depend on the gate voltage as expected. The slope and the I-V relationship can be seen from the graph for both type of illumination on FET and the different gate voltages. The gate voltage at high 25V creates some leakage current obviously which can be seen even at no drain-source voltage applied. As mentioned with the applied gate voltage the current through the channel did not reach at great values and thus the effect of the threshold voltage is not clearly visible. The recent studies reported the channel current in 100^{th} order of μA, but the samples reach only tens

of that.

Parameter#2 T=350-500C, P=0.1mBar, Substrate#2. Next FET was fabricated on a different substrate at three different growth parameters. As we use the 2nd substrate where the ZnO layer is deposited at two different temperatures, and the idea is to facilitate the deposition in

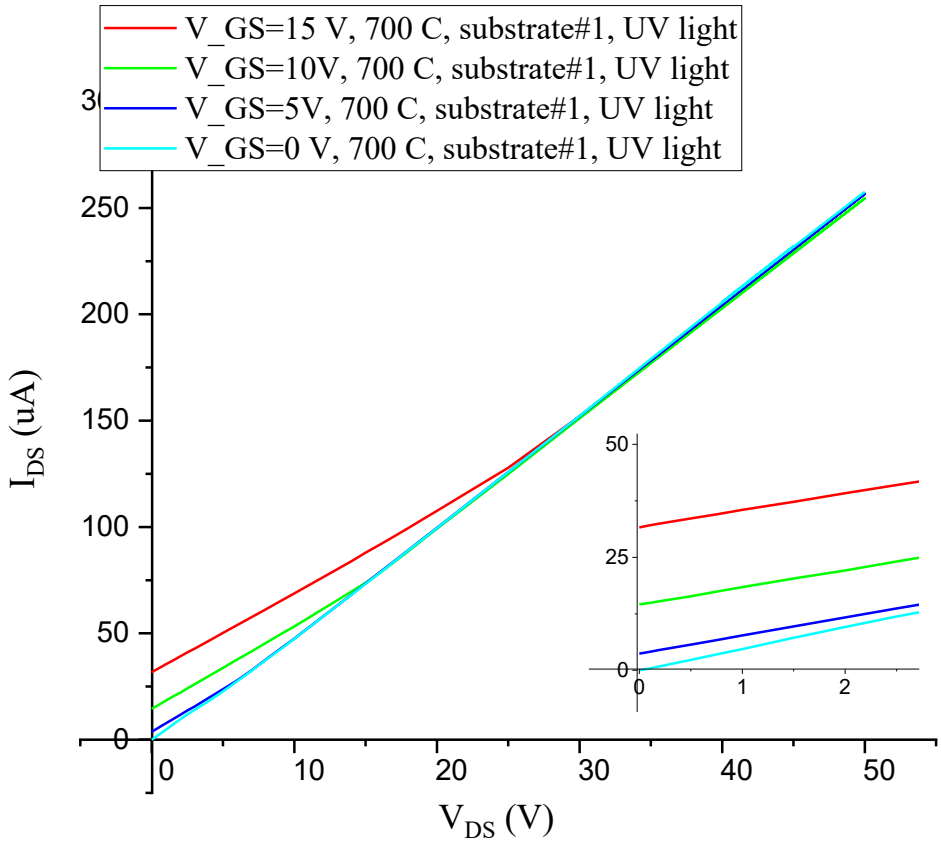

Figure 44: I_{DS}-V_{DS} of 700 C sample for different channel voltage in UV light (μA Vs Volt)

a better way. The initial layers are deposited for a high temperature of 500 C for 20% of the shots and then the rest of the layer is grown at a lower temperature of 350 C for better crystallinity. If we study the current voltage characteristics, we can observe (figure-45,46) that the drain and source current is following the almost same pattern as the previous one. The magnitude is

different, but the thin film experienced a switch on effect as the gate voltage is applied and increased. At two different voltages applied in the drain-source terminals and the effect is studied. As the gate voltage is applied from a negative -10V to around 25V, the channel had a steady 0.4 µA and 1.2 µA current at absence of proper gate voltages for 1V and 3V of drain-source voltages, respectively.

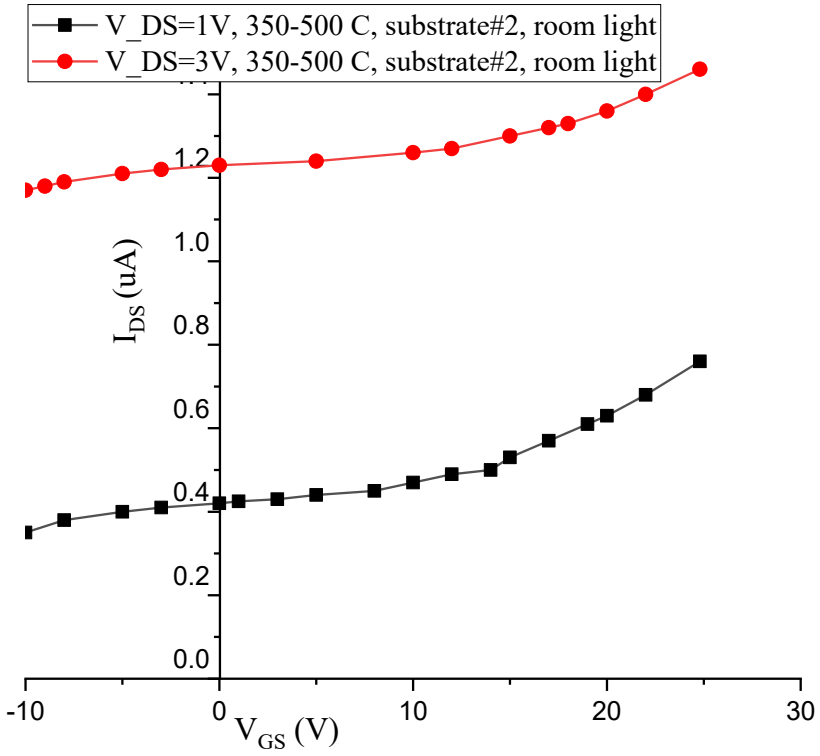

Figure 45: I_{DS}-V_{GS} of 350 C sample for different channel voltage in room light (µA Vs Volt)

Now as the gate voltage increases, the channel at a critical point is apparently switched on and experience a higher increase of current as the voltage is applied for the same drain-source voltage. The switch-on voltages are not the same for the two different channel terminal voltages as the previous sample as it is shown below. We can observe that the table-11 shows that the extra lighting does not impact the performance of the FET channel, and the switch on voltages

are the same for both strong and room lights. Again, the on voltages at the gate is quite high, and on the other hand the current passed is quite low in magnitude. This can be a low current FET, but the voltage requirement being a little high makes it an almost same power device.

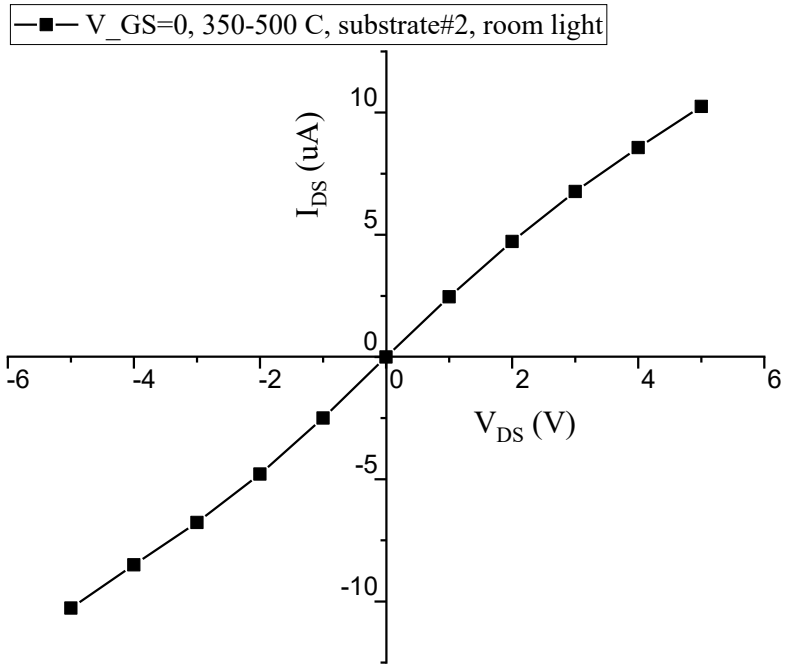

Figure 46: I_{DS}-V_{DS} of 350 C sample for different channel voltage in room light (μA Vs Volt)

Table 11: On voltage required at the gate for 350 C sample in different light exposition

	UV light applied	UV light not applied
V_{DS}=1 V	13 V	13 V
V_{DS}=3 V	17 V	17 V

The I-V characteristics are shown in the figure-46 as the gate voltage of 5 V applied and the plot shows an almost ideal ohmic characteristics (figure-46). It starts with a zero-channel current as the voltage applied across drain-source is zero and it rises in a linear fashion as the

voltage is increased. The resistance of the channel at this gate voltage is around 1MΩ for the whole range of positive and negative voltage alike. It does not approach the saturation obviously that an ideal FET should, but the current seems to gradually decrease as the V_{DS} is increased. The pattern shows that at around 6V the channel has a substantial loss in slope in the I-V plot. The plot being start from the origin indicates the low leakage current of the gate as no significant channel current flows as the gate voltage or light is being applied (table-12). Only when in presence of the gate voltage the drain-source voltage is applied, the channel conducts current.

Parameter#3 T=500C, 30 Minutes Annealed, P=0.1mBar, Substrate#2. The next FET (figure-47,48) was grown steadily at 500 C and then it was annealed for a while (30 mins) in the

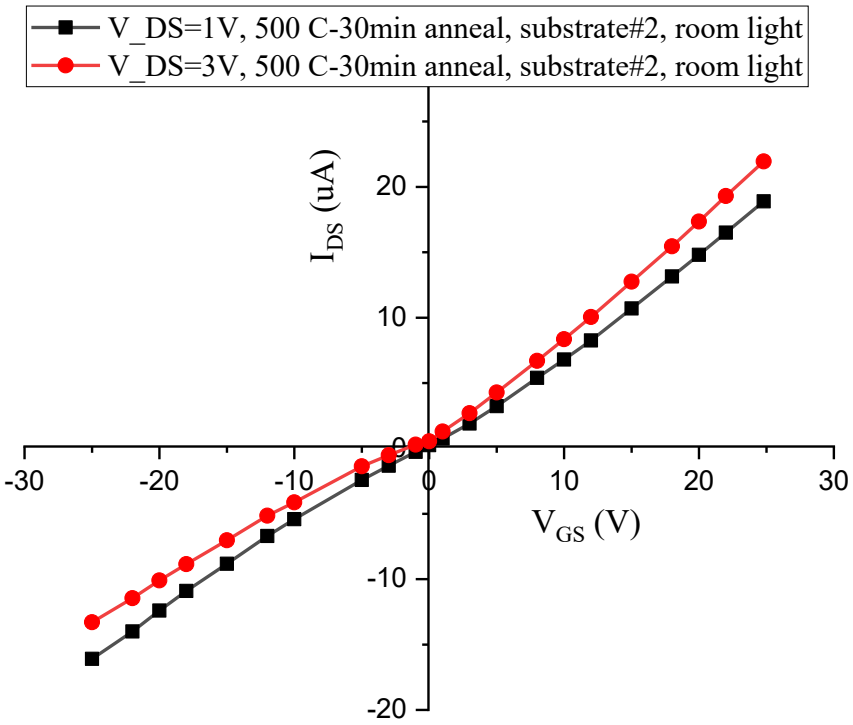

Figure 47: I_{DS}-V_{GS} of 500 C sample (annealed) for different V_{DS} in room light (µA Vs Volt)

same temperature. As the previous sample the terminal of the channel was of 1V and 3V and the

gate voltages were swinging in a 30V range both sides. The nature of this device under this current-voltage experiment shows different behaviour than the previous ones as it has a remarkably high on-off characteristics with no apparent saturation as the gate voltage rises. Multiple samples are fabricated under the mentioned conditions and the gate voltage shows severe impact on the channel. Apparently, the channel is on from the very onset of the gate voltage application. If we consider the off voltage as 0V and as the saturation is not achieved, even after 30V application, we can assume that the saturation should be around or above 50V and the on-off ratio of the FET should be very high as the industry standard. Again, the off

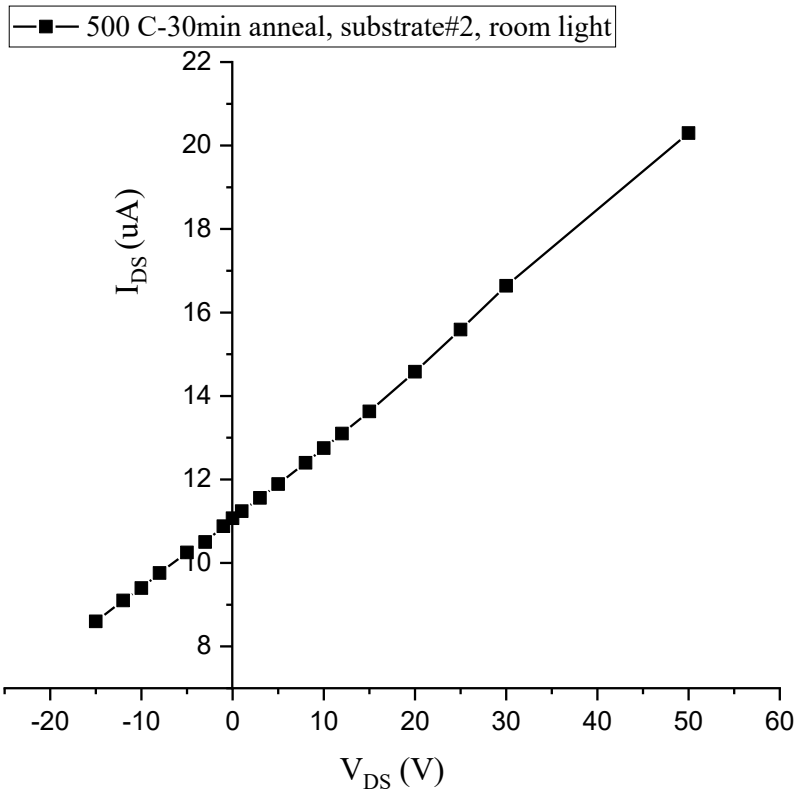

Figure 48: I_{DS}-V_{DS} of 500 C sample (annealed) for different V_{DS} in room light (µA Vs Volt)

voltage is probably very low at around tens of mV range which is not desired and actually

unusable as per the device requirement. Because if we compare the on voltage of tens of Volts magnitude, the off voltage makes the FET a poor one. The I-V characteristics of the channel is given here for this sample. As discussed, the channel shows a typical ohmic response because of the channels state of being 'on' as the gate voltage applied. The plot has a gat voltage of 3 volt and as expected the channel carries the current as voltage is applied across the terminals of drain and source. Another issue regarding this I-V plot is that the expected saturation as it should be for an FET drain-source channel is not present here. All the samples fabricated for FET performances; it showed a pretty straight ohmic response with an impedance of 5.5 MΩ with no probable saturation as the applied DS voltage reached over 50V. As the experiment shows, the material is not suitable for fabricating an FET as it shows. There is also leakage current present as the gate voltage applied with no drain-source voltage applied and still ~10 μA current flows. Compared to the increment of channel current, the initial leakage current is high and the loss in this device due to off/leakage current will be high thereby.

Parameter#4 T=500 C No Anneal, P=0.1mBar, Substrate#2. Now, this is the last sample of the FET (figure-49) in this study where the drain current is low, and a salient on characteristics can be noticed as the drain current increases at a certain point as the gate voltage is rising. Around 10V of gate voltage at low drain-source voltage (=1V) and a gate voltage of 15V for a higher (=3 V) of drain-source voltage turns on the FET. The whole range of gate voltage of 25V swing in both sides shows different response as the expected positive voltage at gate turns on the channel. The low positive and full negative range of voltage at gate result into low drain-source current in positive and negative values. This shows a good response as an FET for this ZnO layers grown in this mentioned parameter.

The light sensitivity is also absent here as the strong UV light is applied and the result

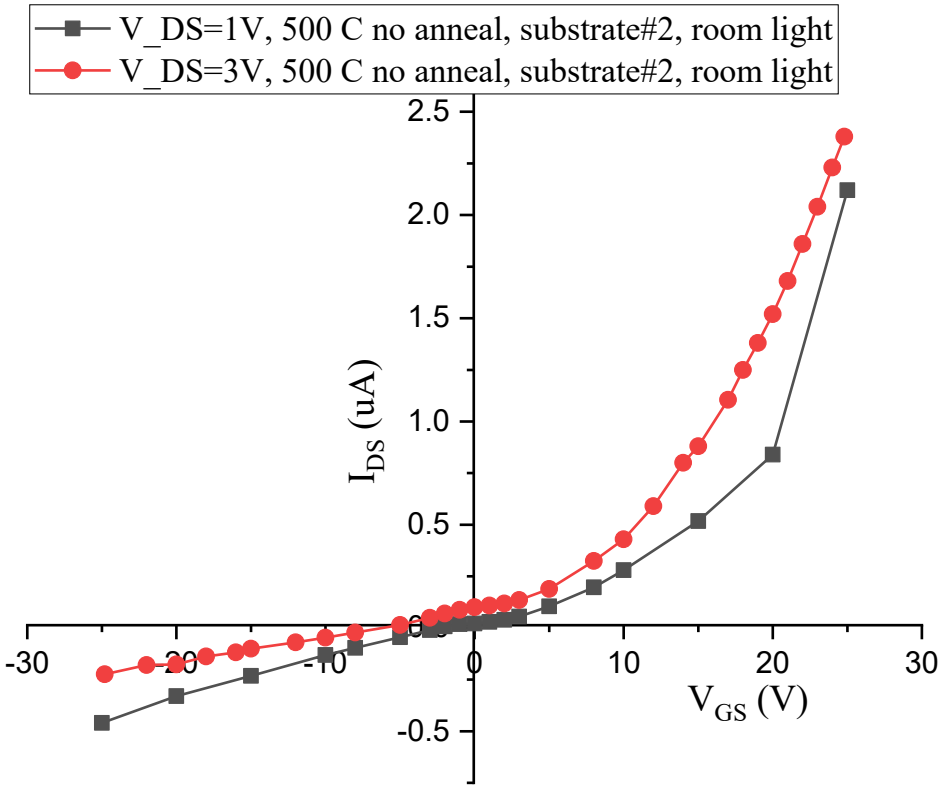

Figure 49: I_{DS}-V_{GS} of 500 C sample (not annealed) for different V_{DS} in room light (µA Vs Volt)

shows the same as the room lighting and it means there is no effect photosensitivity of this FET. The amount of current is remarkably low as it is in the order of µA range and for the same gate and drain-source voltage, the earlier samples were tens to hundred times large in drain-source current. This renders a scope of fabricating a low power device with the same characteristic nature of switching and amplification of signals.

Again, if we study the I-V plot of this sample, the response is purely ohmic (figure-50). The channel has very few leakages as the gate voltage application of 5V does not create any significant current. This is desirable as in the verge of off-on state, the leakage is practically zero and the off current negligible. Although the on state itself has low values of current, the amount

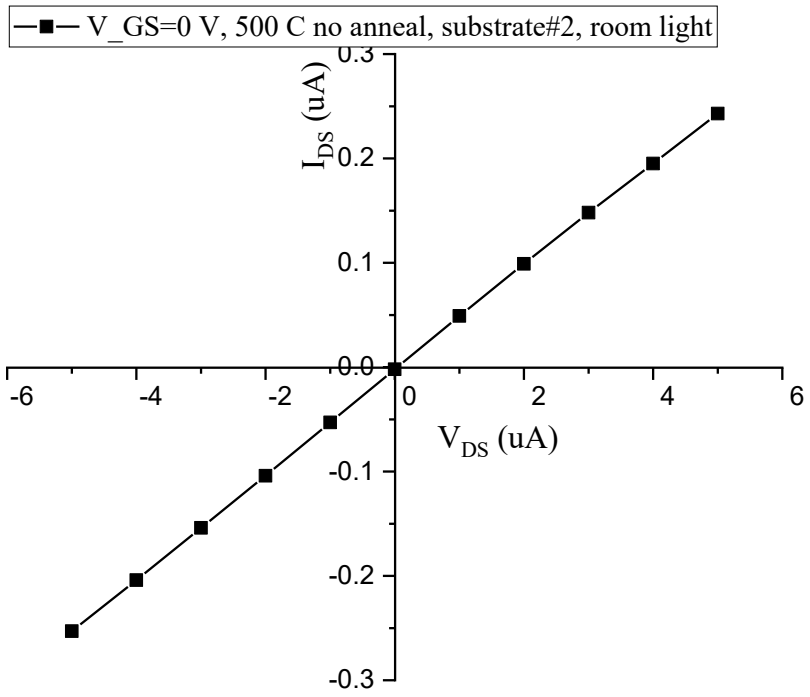

Figure 50: I_{DS}-V_{DS} of 500 C sample (annealed) for different V_{DS} in room light (μA Vs Volt)

of off current still, low compare to that. The I-V plot rises in linear fashion in both positive and negative swing, with a very high impedance of ~20MΩ. This is an extremely high impedance compared to an ideal FET channel which makes it a poor material fabricated for the TFT purpose.

TFT Performance, Carrier Mobility and Light Sensitivity. To measure the performance of a TFT the useful metrics are light sensitivity (figure-51,52), on-off ratio, the voltage of the threshold in the gate impact in TFT, the swing of sub-threshold, and the carrier mobility. For getting the I_{on}:I_{off} the current at below or in the negative zone or the noise level is crucial. The ratio is depended on the ion and the capacitive coupling that is created by the interface semiconductor and the insulator and also the gate. As the value is higher, the switching of the circuits is easier, and this is a good metric of the quality of the TFT. Now comparing the

TFT performance, we can see that the samples grown at 350-500 C and annealed at 500 C failed to act like a good TFT. The gate voltage did not induce any accumulation layer, and the gate voltage also did not impact the channel conductivity either. This is also evident in the quality of the crystallinity in the mentioned samples, where the other successful sample had a 20 times sharper peak at the same plane of preference (002). The comparatively successful sample was the first substrate with a layer ZnO grown at 700 C which had an on-off current ratio of above 50 and the 500 C layer made on second substrate which has a ratio of hundreds.

The TFT of ZnO usually suffers from very large V_{Th} which is around 10-20 V compared to other TFTs. The two good TFTs here has a V_{Th} of around 5-8 V which is good compared to the existing results. The use of SiO_2 is helpful reducing the V_{Th}. On the other hand, the subthreshold swing voltage is quite high, over the range of our operation where the metric is to have it as low as possible. The V_T is positive which confirms the enhancement type FET device [8].

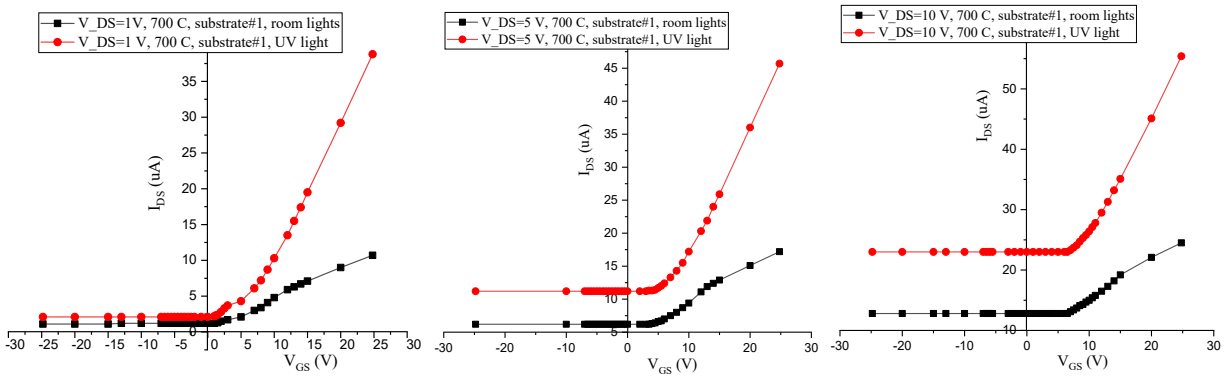

Figure 51: Light sensitivity of 700 C sample for different V_{DS} and gate voltage (µA Vs Volt)

The mobility of the usual TFT ZnO is around 150 cm^2/V-s [8]. It can be measured using the width, length of the TFT channel and measuring the capacitance per area. Using the

transconductance value we can measure the mobility of the TFT device with a good approximation. Using the literature and the experimental values, the calculation is shown in the Table-13 [12].

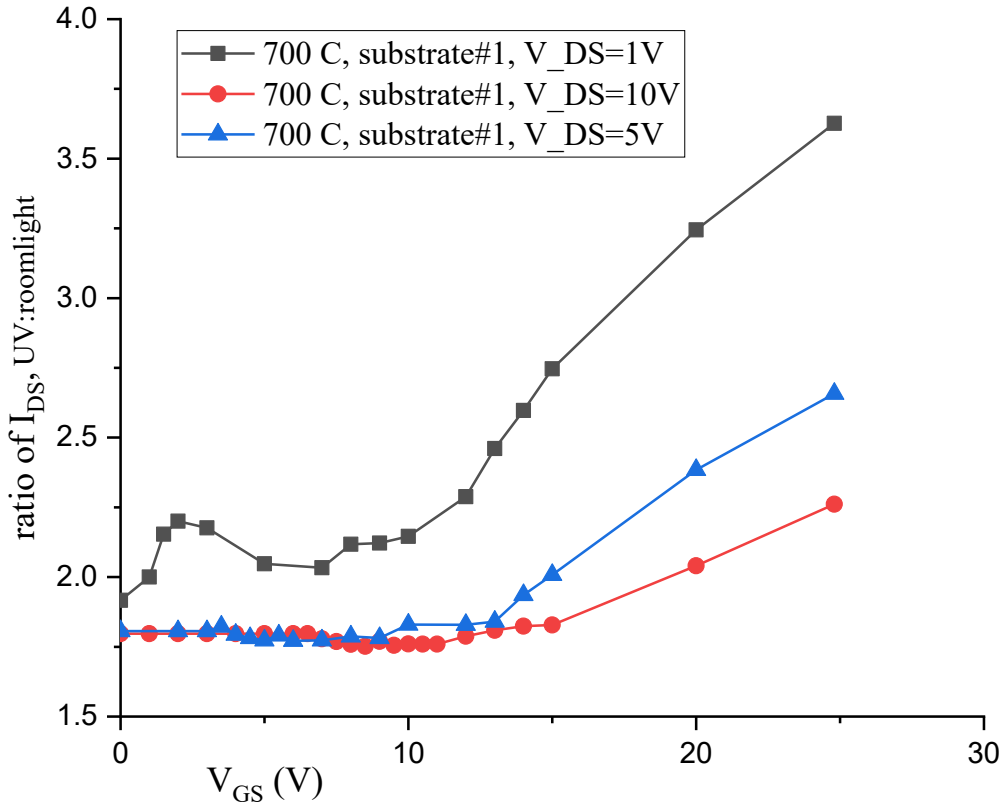

Figure 52: Change of light sensitivity for 700 C sample for different gate voltage (Volt)

Table 12: On voltage required at the gate for 500 C sample in different light exposition

	UV light applied	UV light not applied
V_{DS}=1 V	10 V	15 V
V_{DS}=3 V	15 V	15 V

As expected, the UV illuminated TFT showed higher mobility of 113 $cm^{2/}$V-s, and the

room illuminated TFT was low 62.12. The 500 C sample had a mobility of low 28.24 as expected from the low value of the drain current in the electrical characterization. The TFT that has the ZnO layer grown on the older substrate and had the thin film deposition grown at 700 C showed somewhat light sensitivity and it might also have impacted the performance and output of the FET.

Table 13: Calculation of the carrier mobility

TFT sample	W/L	g_m= slope of sqroot I_{DS}-V_{GS} ($A^{1/2}$/V)	C_{ox}(F/cm^2)	V_{DS}(V)	Mobility (cm^2/V-s)
700 C, substrate#1, room	0.3	0.11	1180.53	5	62.12
700 C, substrate#1, UV	0.3	0.2	1180.53	5	112.94
500 C, substrate#2	0.3	0.05	1180.53	5	28.24

The impact of gate voltage on the channel current was measured for different drain-source voltages and under two different illumination. As it turns out the ratio of the channel current under UV strong light and room light depends on the gate voltage and the applied voltage between drain and source terminals. In Figure-52 we can notice this. While calculating the transconductance, the average of the slope was taken for the I_{DS}. Hence, considering the on-off ratio, the 500 C sample is superior while in mobility, the 700 C film showed better results.

CONCLUSIONS

The fabrication of the ZnO based thin film transistor on two different substrates was done in this study. The structure of the thin film transistor (TFT) was a bottom gate co-planar TFT, one of the most popular method for making. The ZnO was used as the semiconductor material and was grown at different temperatures as mentioned in the study while keeping the pressure same to keep the study understandable in this limited thesis. The main project was devised as to make a good quality TFT using the existing facility for different growth parameters and establish a complete matrix for ZnO TFT performance over a range of different parameters. The time constraint hindered the completion of the project and hence the study is a fraction of the original plan. The sample number of presentable-quality TFT is only four and the pressure was not varied. Moreover, there was a plan of inclusion of a high dielectric constant material (preferably HfO_2 or $BaTiO_3$) between the substrate and the semiconductor (using PLD) for a better threshold voltage and good on-off ratio. The study eventually consists of the variation of two substrates and four different temperature samples of TFT and their comparison as a TFT along with a study of characterization. The characterization by XRD and the photoluminescence were the keys to the analysis of properties and behavior as the ZnO was not doped for band gap engineering (giving the Raman seemingly same for all the samples), and the EDS displayed a fairly similar composition of elements (Zn, C, Si, O), which is the reason to not include the EDS and Raman analysis in this thesis. The low temperature grown ZnO and the annealed ZnO TFT showed extremely poor performance as showing no accumulation layer as the gate voltage applied and produced an ohmic response in the electrical tests. On the other hand, the ZnO grown at 500 C without annealing gave a better response. The study on lightly doped (higher resistivity)

substrate with a higher temperature ZnO thin film showed higher mobility as expose to stronger light which could be a great topic to study in the future. The highly doped substrate having 500 C grown ZnO as semiconductor shows no response to exposed light and hence is insensitive to light. The overall mobility is lower than the ideal value, but it is still in the same order. The TFT was made using an n-type semiconductor (which the ZnO naturally is) which was confirmed by the positive threshold voltage. The on-off ratio is below the expectation which is the probable effect of not using a dedicated and thoroughly clean environment for the growth of the semiconductor and also the high contact resistance due to the gold sputtered electrodes as the source and drain. The electrical characterization setup was able to provide not more than 30 volts because of the bad voltage regulation of the source and moreover, higher gate voltage caused some damage on the film. This impacted the study and the achievement of a full display of current saturation of the TFT channel. This phenomenon should also be delved into to understand the probable cause of this impairment of the experimental set-up and the film capacity (probably improving the electrode fabrication technique and better electrical design of the setup). This study showed a possibility of studying the thin film semiconductor to study the impact of growth parameters of the semiconductor material (ZnO) and the impact of the inclusion of various high dielectric material ($BaTiO_3$, HfO_2). As with the improved electrical characterization and fabrication technique the TFT study can provide a lot of new discoveries regarding the TFT performance for the variables. This thesis is not a comprehensive study on this topic, but it will give some insight and lead to the further research on thin film transistor of ZnO and its derivatives in the near future.

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